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Design and Implementation of a Modified Boost Topology with High Voltage Ratio and Efficiency Besides the Lower Semiconductors Stresses

Reza Sharifi Shahrivar[1], Hossein Gholizadeh[2,*], Alireza Siadatan[1], Ebrahim Afjei[2]

[1] *Electrical engineering faculty of Islamic Azad University , Tehran, Iran*
[2] *Department of Electrical Engineering, Shahid Beheshti University, Tehran, Iran*

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ABSTRACT

This paper has designed an upgraded form of the boost topology. The voltage ratio of the traditional step-up topology has been increased in quadratic form. Moreover, a low value of the duty cycle, number of components, and voltage/current stresses besides a high efficiency are bold features. The different parameters have been extracted for the ideal/non-ideal modes of the components and continuous/discontinuous current modes. In addition, the different features, such as the current/voltage stresses, have been compared. The efficiency of the designed topology has been extracted, and its various kind of power losses have been compared. The small-signal analysis has been done, and the bode diagram of the system has been extracted. Besides the increased voltage ratio of the designed topology compared to the traditional step-up converter, the continuity of the input current has remained a brilliant feature. Moreover, the semiconductors' stresses have been low-value compared to the recently proposed topologies. Moreover, higher efficiency besides higher voltage gain has been achieved. Finally, the experimental results have been compatible with the simulation and theoretical outcomes. The higher voltage gain of the proposed converter has been caused by the lower value of the duty cycle in comparison with the conventional boost converter, besides an acceptable efficiency and semiconductor stresses.

1. Introduction

With the pass of time, the new gates of science have been opened by the researchers to develop technology, simplify the industrial process, increase efficiency, reduce costs, and make human life more straightforward than in the past [1], [2], [6], [8]. Power electronics and the use of semiconductor devices are new fields that have been effective in power generation, transportation, a new generation of lamps, space satellites, distributed power generation, and daily life applications. DC-DC converters are another widely employed equipment in renewable energy applications, uninterruptible power supplies, electric cars, and new light bulbs [1],[2]. Generally, the DC-DC topologies are divided into two main groups: transformer-based and transformer-less DC-DC converters. Increasing the voltage ratio is quickly done by the isolated DC-DC topologies [2], [4], [5]. In other words, the voltage ratio can be changed by the winding ratio and duty cycle [2], [6]. It should be noted that the use of a high-frequency transformer is not without its drawbacks [4]- [8]. The saturation of the transformer core, EMI problems due to the leakage inductors, low efficiency, high voltage stress of switches, cost, and volume are some of the problems that have been caused by the transformer-based DC-DC topologies [4]- [8]. For this reason, the transformerless DC-DC topologies are used to solve the problems of DC-DC isolated converters. The simplest

* Corresponding author
E-mail address: ho.gholizadeh@mail.sbu.ac.ir
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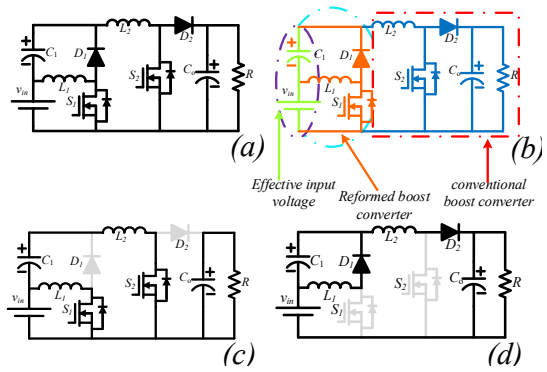

Fig. 1. **(a)** The proposed converter, **(b)** different parts of the proposed converter, **(c)** the equivalent circuit of the first mode, **(d)** the equivalent circuit of the second mode.

topology of non-isolated converters with the step-up behavior is the boost converter [4]-[8]. The topology of the mentioned converter comprises an inductor, a diode, a switch, and an output capacitor. The small components number of the mentioned converter is an advantage of the mentioned converter. It is worth noting that the boost converter has its limits. In other words, it is not possible to reach the desired high voltage gain by the mentioned converter. It is good to mention that the reverse recovery problems and the parasitic components of the devices are effective in the mentioned concept. As a result, modified and new structures must be used to achieve high voltage ratios [8].

In [9]-[17], new typologies of the DC-DC converters have been proposed. Quadratic buck-boost converters have been proposed in [9]- [13]. All the mentioned converters can operate as step-up/down and pass-through converters. The input current of [10], [13] are discontinuous. Therefore, the input filter capacitor will be increased and experience high current stresses. The number of storage components in [9], [11], [12] is high and can increase the dimension of the topology. Moreover, the voltage stress of semiconductor devices is high [12]. The voltage ratio of the proposed converters in [14], [15] is a multiplication of the voltage ratio of conventional boost and buck-boost topologies. The high number of storage components is a disadvantage in the mentioned converters. Moreover, the voltage stress of the second diode is high in both converters. Furthermore, a duty cycle with a 50 percent value makes the output voltage twice the input voltage. In other words, they operate as the conventional boost converter. Another step-up converter has been proposed in [17]. While the duty cycle becomes 50 percent, the output voltage becomes three times more than the input voltage. However, the voltage/current stresses of semiconductor components are high, decreasing the efficiency even with the mentioned advantages.

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In this paper, it has been tried to achieve a high voltage gain by an upgraded form of the conventional boost topology. The voltage ratio of the designed topology is a quadratic form of the voltage ratio of the conventional boost topology. Moreover, a lower number of devices have achieved the mentioned voltage ratio. Furthermore, the continuity of the input current has been kept. Therefore, it is compatible with renewable energy resources. Moreover, it has been tried to have low and acceptable semiconductor voltage/current stresses besides its high voltage ratio. Therefore, the efficiency of the designed topology has an acceptable and high value. The bolded feature of this topology is its voltage-increasing technique. In other words, the summation of the input source voltage and the first stage capacitor helps the second part of the converter to have a higher voltage at the output terminal. Therefore, the voltage stress of the capacitor decreases, and it is not required to employ a capacitor with a high nominal voltage. It is worth noting that the mentioned concept has not been obeyed in the suggested converters of [9]- [17].

2. The introduced topology

The topology of the designed converter has been illustrated in Fig. 1(a). As can be understood from Fig. 1(b), the designed topology combines two conventional boost converters. As shown in Fig. 1(b), the first stage of the proposed converter has been designed to increase the input voltage of the second part. In other words, the first part has made an effective input voltage for the second stage. Moreover, the input voltage decreases the applied voltage of C1. In other words, the input voltage participates as the input of the second part and the first capacitor voltage. All the mentioned concepts and their creation procedure can be understood in Fig. 1(b). Both the switches in the proposed converter become turned ON and OFF synchronously. The conduction of diodes takes place during the switches are turned OFF. Consequently, two function modes can be considered for the proposed circuit. All the circuit components have been considered ideal for simplifying the study of the suggested converter. Moreover, it has been accounted that the converter

operates in the steady-state and the continuous current mode (CCM).

2.1. The first operation mode

During the first function mode, both the MOSFETs become ON. Consequently, both diodes become OFF. The appropriate circuit of this mode has been presented in Fig. 1(c). Both the inductors are magnetized by the capacitors and the input voltage, caused by their positive voltage. Moreover, the capacitors become discharged, caused by their negative current. The mentioned concepts have been expressed mathematically by (1):

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = v_{in}, L_2 \dfrac{di_{L2}}{dt} = v_{in} + v_{c1} \\ C_1 \dfrac{dv_{C1}}{dt} = -i_{L2}, C_o \dfrac{dv_{Co}}{dt} = -I_o \end{cases} \quad (1)$$

2.2. The second operation mode

In this mode, both the MOSFETs are OFF. Therefore, both diodes become ON. The equivalent circuit of the forenamed mode has been presented in Fig. 1(d). The inductors become demagnetized due to their negative voltage in the mentioned model. Moreover, the positive current of capacitors causes their charging in the second mode. The expressing relations of the inductors voltage and capacitors current in the present mode are as (2):

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = -v_{c1}, L_2 \dfrac{di_{L2}}{dt} = v_{in} + v_{c1} - v_{co} \\ C_1 \dfrac{dv_{C1}}{dt} = i_{L1} - i_{L2}, C_o \dfrac{dv_{Co}}{dt} = i_{L2} - I_o \end{cases} \quad (2)$$

2.3. The average of the capacitors voltage and inductors current

The voltage second balance refers to a zero average voltage of inductors. Therefore, by applying the mentioned concept to both relations of the inductors' voltage during both of the operation modes, the average value of the capacitors' voltage can be written as:

$$V_{C1} = \frac{D}{1-D} V_{in}, V_{Co} = \frac{1}{(1-D)^2} V_{in} \quad (3)$$

Employing the average voltage of the capacitors, the voltage gain of the mentioned converter has been written as (4):

$$\frac{V_{Co}}{V_{in}} = \frac{1}{(1-D)^2} \quad (4)$$

The Dual of the last concept can be applied to the capacitors. In other words, the current second balance refers to the zero average currents of capacitors. Consequently, applying this concept to the current relations of capacitors for both of the operation modes, the average current of the inductors can be formulated as (5):

$$I_{L1} = \frac{1}{(1-D)^2} I_o, I_{L2} = \frac{1}{1-D} I_o \quad (5)$$

2.4. Voltage/current stress of semiconductors

The average voltage which is applied to the semiconductor devices by the capacitors, and input voltage and their average current are as below:

$$V_{S1} = V_{D1} = \frac{V_{in}}{1-D}, V_{S2} = V_{D2} = \frac{V_{in}}{(1-D)^2} \quad (6)$$

$$I_{S1} = \frac{D}{(1-D)^2} I_o, I_{S2} = I_{D1} = \frac{D}{1-D} I_o, I_{D2} = I_o \quad (7)$$

2.5. Capacitors voltage ripple and inductors current ripple

The capacitors' voltage ripple refers to the subtraction of the maximum and the minimum value of the voltage waveform. It is worth noting that the value of the voltage ripple depends on the amount of the capacitors. The dual of the mentioned concept can be expressed for the inductors. The inductors' current ripple refers to the difference between the maximum and minimum amounts of the inductors' waveform. The capacitors' voltage gain and inductors' current ripple have been expressed as (8):

$$\begin{cases} \Delta V_{C1} = \dfrac{DI_o}{(1-D)C_1 f_s} \\ \Delta V_{Co} = \dfrac{DI_o}{C_o f_s} \end{cases} \quad \begin{cases} \Delta I_{L1} = \dfrac{DV_{in}}{L_1 f_s} \\ \Delta I_{L2} = \dfrac{DV_{in}}{(1-D)L_2 f_s} \end{cases} \quad (8)$$

3. Discontinuous conduction mode

The converter operating in CCM depends on the inductors' average current and inductors' current ripple. The inductors' average current decreases to less than half of the corresponding inductor's current ripple, concluding the discontinuous conduction mode (DCM). The inductors' average current depends on the average output current. (9) defines the border value of the output current for the constant input and output voltage.

$$\begin{cases} I_o = \dfrac{DV_{in}}{2L_2 f_s} \\ I_o = \dfrac{D(1-D)^2 V_o}{2L_2 f_s} \end{cases} \quad (9)$$

It is good to note that the calculated output current according to (9) defines the boundary value of the output current between CCM and DCM. If the output current were less than the calculated values by (9), the converter operates in DCM. Otherwise, the operation takes place in the CCM region.

The increase of the current ripple to more than the twice of the average current concludes the converter's operation in the DCM. Therefore, the minimum value of the inductors has been discussed as (10).

$$\begin{cases} L_1 > \dfrac{D(1-D)^4 R}{2f_s} \\ L_2 > \dfrac{D(1-D)^2 R}{2f_s} \end{cases} \quad (10)$$

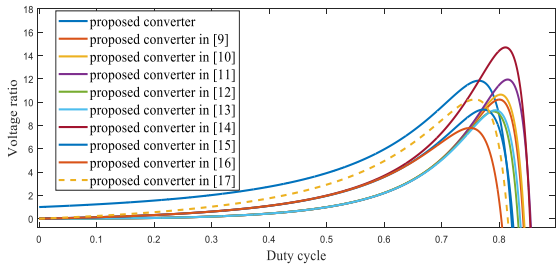

Fig. 2. The comparison of the non-ideal voltage gain of the proposed and recently suggested topologies.

4. The improvements

4.1. Non-ideal voltage gains of the suggested converter and conventional converter as a point of view

Due to the non-ideal state of the circuit components, DC-DC converters cannot operate according to their ideal voltage ratio. The relation of the voltage ratio in non-ideal mode has been expressed to visualize the capability of the proposed converter compared with the conventional step-up topology as below:

$$\frac{V_O}{V_{in}}=\frac{1}{(1-D)^2}-\frac{r_L}{R}F_1(D)-\frac{r_{SD}}{R}F_2(D)-\frac{r_D}{R}F_3(D) \quad (11)$$

$$\begin{cases} F_1(D)=\dfrac{D^2-2D+2}{(1-D)^6} \\ F_2(D)=\dfrac{D^3-2D^2+2D}{(1-D)^6} \\ F_3(D)=\dfrac{D^2-2D+2}{(1-D)^5} \end{cases} \quad (12)$$

The corresponding plots of the mentioned relations have been plotted and illustrated in **Fig. 2**. With an approximation, all the mentioned coefficients r_L, r_S, and r_D have been assumed the same. It is good to note that the mentioned parasitic components belong to the equivalent series resistance of the inductors, switches, and diodes. As shown in Fig. 2, the maximum amount of the non-ideal voltage ratio is 12. Additionally, the maximum voltage gain of the boost converter has been extracted 12 according to the mentioned figure. However, the corresponding duty cycle to the maximum voltage gain of the boost converter is higher than the same one in the suggested topology. Consequently, the proposed converter provides a higher value of the voltage gain by a lower duty cycle value. It is worth noting that the higher value of the voltage gains in the boost converter by relative values of the duty cycle to unity makes its diode suffer from reverse recovery problems besides the dramatic voltage/current stresses. Moreover, The topology of the proposed converter has employed two traditional Boost topologies. The first one has been deformed to employ the input voltage directly in increasing the voltage gain. In other words, the summation of the input voltage and the first capacitor act as a modified input source for the second part. Moreover, the voltage stress of the first capacitor is less than the corresponding capacitor in the cascaded boost topology.

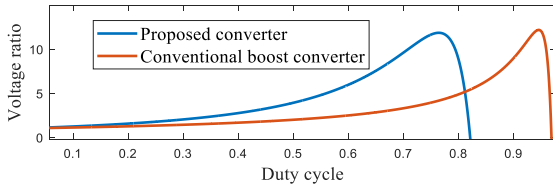

Fig. 3. The comparison of the non-ideal voltage gain of the proposed and recently suggested topologies.

4.2. Non-ideal voltage gains of the suggested converter and suggested converters in [9]-[17] as a point of view

To confirm the capability of the mentioned topology among mentioned converters of [9]- [17], the non-ideal the voltage gain of the presented converters has been compared and illustrated in Fig. 3. Except for the presented converter in [14], all cases have a lower value of maximum voltage gain than the proposed topology. The maximum amount of the voltage ratio of the mentioned topology of [14] has taken place in a duty cycle, which causes poor efficiency. All the non-ideal voltage gain curves in Fig. 3 have been extracted with some assumptions such as:

- All the parasitic components that become apparent with the non-ideal voltage ratio of converters have been assumed to be the same.
- All the plots have been extracted for 80 W output power.

As can be understood from Fig. 3, the maximum voltage gain of the proposed converter in the same conditions for all has achieved an acceptable and high value. Moreover, as the duty cycle varies from 0 to the corresponding value of the duty cycle to its maximum point in the suggested converter, the voltage gain of this converter is higher than the others. All the plots have been extracted for 80 W output power.

4.3. The comparison of the different features and the parameters

The various features and parameters of the presented topology have been compared with the mentioned converters of [9]- [17] in Table I to confirm the advantages of the presented topology. In the proposed converter and the mentioned converters in [10], [13], [16], [17], there are two inductors and capacitors. The number of the mentioned components is 3 in the proposed converters of [9], [11], [12], [14], [15]. The number of the semiconductor devices is the same in the proposed and the mentioned converters of [9]- [17]. The input current continuity makes the DC-DC converters suitable for renewable applications by reducing the input filter capacitor value. As can be understood, the input current of the designed topology is continuous like the proposed converters of [9], [11], [12], [14]- [17]. The duty cycle value, which causes the voltage gain of 4, has been

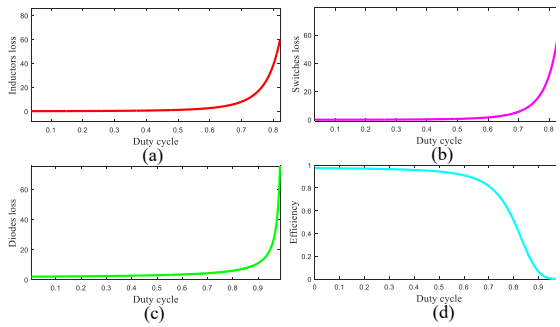

Fig.4. (a) Inductor loss, (b) switch loss, (c) diode loss, (d) efficiency.

calculated for the proposed and mentioned converters of [9]- [17]. Compared with [9]- [17], the proposed converter needs a lower amount of the duty cycle. The semiconductors' normalized voltage/current stresses have been explained according to the corresponding duty cycle of each converter. As can be understood, the normalized value of the voltage stress of the first switch in the designed topology has the lowest value. By exception of the proposed converter of [15], the voltage stress of the second switch of the designed one is lower than the mentioned converters of [10]- [14],
[17]. The mentioned parameter has the same value in the proposed converters of [9], [16]. Moreover, the normalized value of the voltage stress of the first diode in the suggested topology has the lowest value among the mentioned converters of [9]- [17] as well as the second one has the lowest value among the mentioned converters of [9]- [14], [17]. It has to be announced that the voltage stress of the second diode in the presented topology is the same as the mentioned topologies of the rest. The current stress of both switches in the designed converter has achieved the lowest value among the mentioned converters of [9]- [17]. The current stress of the first diode in the designed topology has the same value as the mentioned converters of [9]- [13], a lower value than the mentioned converters of [15]- [17]. It has a higher value in comparison with [14]. The normalized current stress of the second diode has the same value in all the discussed and the proposed converter approximately. It is worth noting that the voltage of the output capacitor and input current are the base values to normalize the voltage and current stresses, respectively.

5. Efficiency

The power loss of the inductors, switches, and diodes has been considered to extract the mathematical relation of the efficiency. The power loss of the switches can be divided into conduction and switching loss. To simplify the extracted relation, the foko and hysteresis losses of the inductors and frequency loss of the diodes are neglected. All the mentioned types of the loss have been described below:

5.1. Inductors conduction loss

The conduction loss of the inductor is the production of the equivalent series resistance of the inductor with the quadratic form of its current RMS value.

$$P_L=\left\{I_{L1}^2 r_{L1}+I_{L2}^2 r_{L2}\right\}=\left\{\frac{1}{(1-D)^4}r_{L1}+\frac{1}{(1-D)^2}r_{L2}\right\}\frac{P_o}{R} \quad (13)$$

5.2. Conduction loss of switches

The switches' conduction loss is the production of the equivalent series resistance of the switch with the quadratic form of the RMS value of the current.

$$P_{SC}=\left\{I_{S1}^2 r_{SD1}+I_{S2}^2 r_{SD2}\right\}=\left\{\frac{D}{(1-D)^4}r_{SD1}+\frac{D}{(1-D)^2}r_{SD2}\right\}\frac{P_o}{R} \quad (14)$$

5.3. Switching loss of switches

The switches' switching loss is half of the production of the average voltage and current of switches with the frequency and the turn-OFF delay time.

$$P_{SS}=\frac{1}{2}f_s\left\{V_{S1}I_{S1}t_{OFF1}+V_{S2}I_{S2}t_{OFF2}\right\}=\frac{1}{2}f_s P_o\left(\frac{D}{1-D}\right)\left\{t_{OFF1}+t_{OFF2}\right\} \quad (15)$$

5.4. Conduction loss of diodes

The power loss of the diodes is the production of the average current of the diode with its threshold voltage.

$$P_D=V_{DF1}I_{D1}+V_{DF2}I_{D2}=\left\{V_{DF1}\left(\frac{1}{1-D}\right)+V_{DF2}\right\}I_o \quad (16)$$

After calculating the mentioned power losses, the efficiency is as below:

$$\eta=\frac{P_o}{P_o+P_{SC}+P_{SS}+P_D}\times 100\% \quad (17)$$

Fig. 4 presents the mentioned power losses and the efficiency for all duty cycle percentages. The corresponding output power of the plots in Fig. 4 is 80W. As can be understood from Fig. 4(d), the efficiency of the presented topology decreases from 98 % to 80 %. At the same time, the duty cycle varies from 0 to 75 %. In addition, the efficiency of the designed topology becomes 96 % when the duty cycle becomes 50 %. It is worth noting that the mentioned power losses vary from 0.01 W to lower than 10 W, as the duty cycle varies from 0 to 75 %.
Fig. 5 presents the efficiency of the topology for the various output powers and all values of the duty cycle. The efficiency is more than 94%, while the duty cycle varies from 0 to 50 %, and the output power varies from 20 W to 200 W, according to Fig. 5(a). In Fig. 5(b), the duty cycle varies from 50 % to 100 %. The efficiency is more than 80 percent for all the mentioned output power values, while the duty cycle is lower than 66 %. While the duty cycle varies to 75 %, only for the output power of 20W to 80 W, the efficiency is more than 80 %.

In Table 2, the mentioned power losses have been compared for the proposed converter and the mentioned converters of [9]- [17] for an amount of the duty cycle,

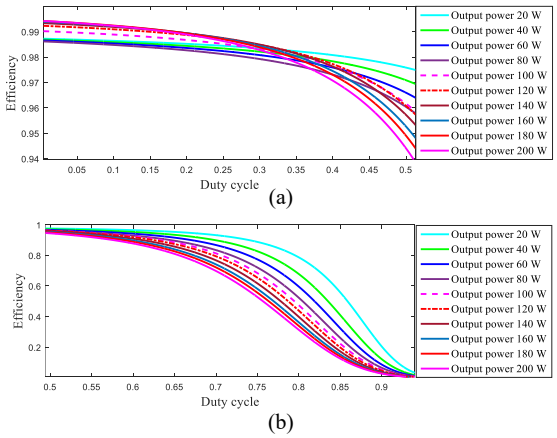

Fig. 5. The efficiency of the converter for the different output powers while the duty cycle varies from(a) 0 to 50 %, (b) 50 % to 100 %.

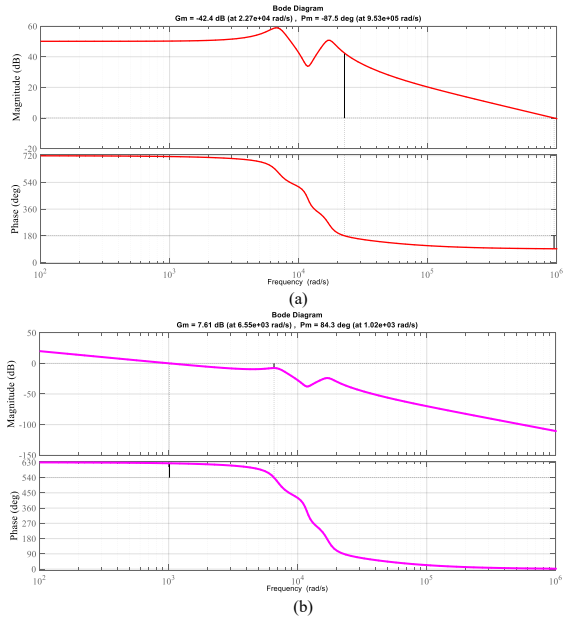

Fig. 6. The bode diagram of the proposed converter: (a) before compensating, (b) after compensating.

causing the voltage gain of 4. The last column of Table 2 belongs to the calculated value of the duty cycle. The second column of Table 2 is for the inductor loss of the mentioned converters. It is good to note that the inductor loss of the proposed converter is lower than [9]- [16]. Moreover, the conduction loss of the switch in the presented topology has the lowest value compared to the

mentioned converters of [9]- [17]. In addition, the switching loss of the proposed converter has achieved the lowest value compared with mentioned converters of [9]-[17]. Finally, the fifth column of the mentioned table compares the diode loss. The value of the diode loss for the proposed converter has the lowest value among the converters of [9]- [13], [15]- [17]. Consequently, the designed converter has a better efficiency among [9]-[17], while the duty cycle causes a voltage gain of 4.

6. Small signal analysis

To study the stability of the proposed converter, the state space variables of the proposed topology and their appropriate relations during both the function modes have been Witten as below:

$$\begin{cases} L_1 \dfrac{d\prec i_{L1}\succ}{dt} = d\prec v_{in}\succ -(1-d)\prec v_{C1}\succ \\ L_2 \dfrac{d\prec i_{L2}\succ}{dt} = \prec v_{in}+v_{C1}\succ -(1-d)\prec v_{Co}\succ \\ C_1 \dfrac{d\prec v_{C1}\succ}{dt} = -\prec i_{L2}\succ +(1-d)\prec i_{L1}\succ \\ C_o \dfrac{d\prec v_{Co}\succ}{dt} = -\prec \dfrac{v_{Co}}{R}\succ +(1-d)\prec i_{L2}\succ \end{cases} \quad (18)$$

All the space state variables can be assumed to be a DC and AC part summation. Moreover, the AC term of the mentioned variables is negligible in comparison with DC terms as below:

$$\begin{cases} \prec i_{L1}\succ = \prec I_{L1}\succ + \prec \hat{i}_{L1}\succ \\ \prec i_{L2}\succ = \prec I_{L2}\succ + \prec \hat{i}_{L2}\succ \\ \prec v_{C1}\succ = \prec V_{C1}\succ + \prec \hat{v}_{C1}\succ \\ \prec v_{Co}\succ = \prec V_{Co}\succ + \prec \hat{v}_{Co}\succ \\ d = D + \hat{d} \end{cases} \quad \begin{cases} \hat{i}_{L1} \ll I_{L1} \\ \hat{i}_{L2} \ll I_{L2} \\ \hat{v}_{C1} \ll V_{C1} \\ \hat{v}_{Co} \ll V_{Co} \\ \hat{d} \ll D \end{cases} \quad (19)$$

The space state equations can be formed as below:

$$\begin{cases} \hat{x} = Ax + B\hat{d} \\ y = C\hat{d} \end{cases} \quad (20)$$

$$\begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{v}_{C1}}{dt} \\ \frac{d\hat{v}_{Co}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{D-1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{D-1}{L_2} \\ \frac{1-D}{C_1} & \frac{-1}{C_1} & 0 & 0 \\ 0 & \frac{1-D}{C_o} & 0 & \frac{-1}{RC_o} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{Co} \end{bmatrix} + \begin{bmatrix} \frac{V_{in}+V_{C1}}{L_1} \\ \frac{V_{Co}}{L_2} \\ \frac{-I_{L1}}{C_1} \\ \frac{-I_{L2}}{C_o} \end{bmatrix} \hat{d} \quad (21)$$

The bode diagram of the offered topology based on the described space state equations has been plotted and presented in Fig. 6(a) to find the stability requirements of the designed topology. According to the illustrated bode plot, the gain and phase margin of the proposed converter are as -42.4 dB at 22.7 kHz and -87.5 deg at 953krad/s. The positive value of the production of the gain and the phase margin is the stability requirement desired in this converter. Matlab software plotted the bode diagram and found the gain and phase margins. Negative values of the phase and gain margins refer to the non-minimum phase characteristics of the proposed deigned and the compensated bode diagram has been presented in Fig. 6 (b).

7. Simulation and experimental results

This section discusses all the simulations and the experimental outcomes. PLECS has got the mentioned results. The inductors' and capacitors' values are required for the simulation. The percentage of the inductors' current ripple and capacitors' voltage ripple have to be valued to find the inductors and capacitors. Based on the

power quality factors, the inductors' current ripple and capacitors' voltage ripple are 30 % and 5 %, respectively. The inductors' average current and capacitors' average voltage have to be found to use the mentioned percentages. The input voltage and output current have to be defined to find the mentioned average values from (3) and (5). The lab equipment limits and safety considerations lead to assuming the input voltage as 20 V and output current as 1 A. It is good to note that the switching frequency is considered 60 kHz due to the capability of the inductors' windings. According to the mentioned concepts the capacitors' average voltage and inductors' current are as (22).

Table I. The comparison of the different features.

	[9]	[10]	[11]	[12]	[13]	[14]	[15]	[16]	[17]	proposed
No. inductors	3	2	3	3	2	3	3	2	2	2
No. capacitors	3	2	3	3	2	3	3	2	2	2
No. switches	2	2	2	2	2	2	2	2	2	2
No. diodes	2	2	2	2	2	2	2	2	2	2
No.	10	8	10	10	8	10	10	8	8	8
Duty cycle	0.67	0.67	0.67	0.67	0.67	0.62	0.62	0.62	0.55	0.5
$\frac{V_{S1}}{V_O}$	$\frac{1-D}{D^2}=0.73$	$\frac{1-D}{D^2}=0.73$	$\frac{1-D}{D^2}=0.73$	$\frac{1}{D^2}=2.23$	$\frac{1-D}{D^2}=0.73$	$\frac{1-D}{D}=0.61$	$\frac{1-D}{D}=0.61$	$\frac{1-D}{D}=0.61$	$\frac{1-D}{D(2-D)}=0.62$	$1-D=0.5$
$\frac{V_{S2}}{V_O}$	1	$\frac{1}{D}=1.49$	$\frac{1}{D}=1.49$	$\frac{1}{D}=1.49$	$\frac{1}{D}=1.49$	$\frac{1}{D}=1.61$	$\frac{2D-1}{D}=0.38$	1	$\frac{1}{D(2-D)}=1.25$	1
$\frac{V_{D1}}{V_O}$	$\frac{1-D}{D^2}=0.73$	$\frac{1-D}{D^2}=0.73$	$\frac{1-D}{D^2}=0.73$	$\frac{1-D}{D^2}=0.73$	$\frac{1-D}{D^2}=0.73$	$\frac{1-D}{D}=0.61$	$\frac{1-D}{D}=0.61$	$\frac{1-D}{D}=0.61$	$\frac{1-D}{D(2-D)}=0.62$	$1-D=0.5$
$\frac{V_{D2}}{V_O}$	$\frac{1}{D}=1.49$	$\frac{1}{D}=1.49$	$\frac{1}{D}=1.49$	$\frac{1}{D}=1.49$	$\frac{1}{D}=1.49$	$\frac{1}{D}=1.61$	1	1	$\frac{1}{D(2-D)}=1.25$	1
$\frac{I_{S1}}{I_{in}}$	1	1	1	1	1	$D=0.62$	$2-D=1.38$	1	$\frac{1}{D(2-D)}=1.25$	$D=0.5$
$\frac{I_{S2}}{I_{in}}$	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\frac{2D-1}{D}=0.5$	$\frac{1-D}{D}=0.5$	$1-D=0.38$	$1-D=0.38$	$1-D=0.38$	$\frac{1-D}{(2-D)}=0.31$	$D(1-D)=0.25$
$\frac{I_{D1}}{I_{in}}$	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$1-D=0.38$	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D(2-D)}=0.62$	$1-D=0.5$
$\frac{I_{D2}}{I_{in}}$	$\left(\frac{1-D}{D}\right)^2=0.24$	$\left(\frac{1-D}{D}\right)^2=0.24$	$\left(\frac{1-D}{D}\right)^2=0.24$	$\left(\frac{1-D}{D}\right)^2=0.24$	$\left(\frac{1-D}{D}\right)^2=0.24$	$\frac{(1-D)^2}{D}=0.23$	$\frac{(1-D)^2}{D}=0.23$	$\frac{(1-D)^2}{D}=0.23$	$\frac{(1-D)^2}{D(2-D)}=0.24$	$(1-D)^2=0.25$
Continuity of I_{in}	Yes	No	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes

Table II. The different losses comparison.

	P_L	P_{CS}		P_D	D
[9]	$\frac{D^4-2D^3+3D^2-2D+1}{(1-D)^4}\frac{P_o r_L}{R}=55\frac{P_o r_L}{R}$	$\frac{2D^3-2D^2+D}{(1-D)^4}\frac{P_o r_L}{R}=34\frac{P_o r_L}{R}$	$f_s P_o t_{OFF}\left(\frac{1+D}{1-D}\right)=5 f_s P_o t_{OFF}$	$V_{DF} I_O \frac{1}{1-D}=3V_{DF} I_O$	0.67
[10]	$\frac{5D^2-6D+2}{(1-D)^4}\frac{P_o r_L}{R}=20.4\frac{P_o r_L}{R}$	$\frac{2D^3-2D^2+D}{(1-D)^4}\frac{P_o r_L}{R}=34\frac{P_o r_L}{R}$	$f_s P_o t_{OFF}\left(\frac{1}{1-D}\right)=3 f_s P_o t_{OFF}$	$V_{DF} I_O \frac{1}{1-D}=3V_{DF} I_O$	0.67
[11]	$\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}\frac{P_o r_L}{R}=46.33\frac{P_o r_L}{R}$	$\frac{2D^3-2D^2+D}{(1-D)^4}\frac{P_o r_L}{R}=34\frac{P_o r_L}{R}$	$f_s P_o t_{OFF}\left(\frac{1}{1-D}\right)=3 f_s P_o t_{OFF}$	$V_{DF} I_O \frac{1}{1-D}=3V_{DF} I_O$	0.67
[12]	$\frac{3D^4-5D^3+7D^2-4D+1}{(1-D)^4}\frac{P_o r_L}{R}=92\frac{P_o r_L}{R}$	$\frac{5D^3-4D^2+D}{(1-D)^4}\frac{P_o r_L}{R}=34.4\frac{P_o r_L}{R}$	$f_s P_o t_{OFF}\left(\frac{D}{(1-D)^2}\right)=6.15 f_s P_o t_{OFF}$	$V_{DF} I_O \frac{1}{1-D}=3V_{DF} I_O$	0.67
[13]	$\frac{2D^2-2D+1}{(1-D)^4}\frac{P_o r_L}{R}=57\frac{P_o r_L}{R}$	$\frac{2D^3-2D^2+D}{(1-D)^4}\frac{P_o r_L}{R}=34\frac{P_o r_L}{R}$	$f_s P_o t_{OFF}\left(\frac{1}{1-D}\right)=3 f_s P_o t_{OFF}$	$V_{DF} I_O \frac{1}{1-D}=3V_{DF} I_O$	0.67
[14]	$\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}\frac{P_o r_L}{R}=23\frac{P_o r_L}{R}$	$\frac{2D^3-2D^2+D}{(1-D)^4}\frac{P_o r_L}{R}=16.4\frac{P_o r_L}{R}$	$f_s P_o t_{OFF}\left(\frac{1+D}{1-D}\right)=4.26 f_s P_o t_{OFF}$	$V_{DF} I_O \frac{1}{1-D}=2.63V_{DF} I_O$	0.62
[15]	$\frac{3D^2-4D+2}{(1-D)^4}\frac{P_o r_L}{R}=33.7\frac{P_o r_L}{R}$	$\frac{2D^3-6D^2+5D}{(1-D)^4}\frac{P_o r_L}{R}=63.5\frac{P_o r_L}{R}$	$f_s P_o t_{OFF}\left(\frac{1+D}{1-D}\right)=4.26 f_s P_o t_{OFF}$	$V_{DF} I_O \frac{1+D}{1-D}=4.26V_{DF} I_O$	0.62
[16]	$\frac{D^2-2D+2}{(1-D)^4}\frac{P_o r_L}{R}=57.22\frac{P_o r_L}{R}$	$\frac{D^3-2D^2+2D}{(1-D)^4}\frac{P_o r_L}{R}=35.5\frac{P_o r_L}{R}$	$f_s P_o t_{OFF}\left(\frac{1+D}{1-D}\right)=4.26 f_s P_o t_{OFF}$	$V_{DF} I_O \frac{2-D}{1-D}=3.63V_{DF} I_O$	0.62
[17]	$\frac{2D^2-2D+1}{(1-D)^4}\frac{P_o r_L}{R}=12.31\frac{P_o r_L}{R}$	$\frac{D^3-2D^2+2D}{(1-D)^4}\frac{P_o r_L}{R}=16.12\frac{P_o r_L}{R}$	$f_s P_o t_{OFF}\left(\frac{1}{(1-D)(2-D)}\right)=1.43 f_s P_o t_{OFF}$	$V_{DF} I_O \frac{1+D}{1-D}=3.4V_{DF} I_O$	0.55
proposed	$\frac{D^2-2D+2}{(1-D)^4}\frac{P_o r_L}{R}=20\frac{P_o r_L}{R}$	$\frac{D^3-2D^2+2D}{(1-D)^4}\frac{P_o r_L}{R}=10\frac{P_o r_L}{R}$	$f_s P_o t_{OFF}\left(\frac{D}{1-D}\right)=f_s P_o t_{OFF}$	$V_{DF} I_O \frac{2-D}{1-D}=3V_{DF} I_O$	0.5

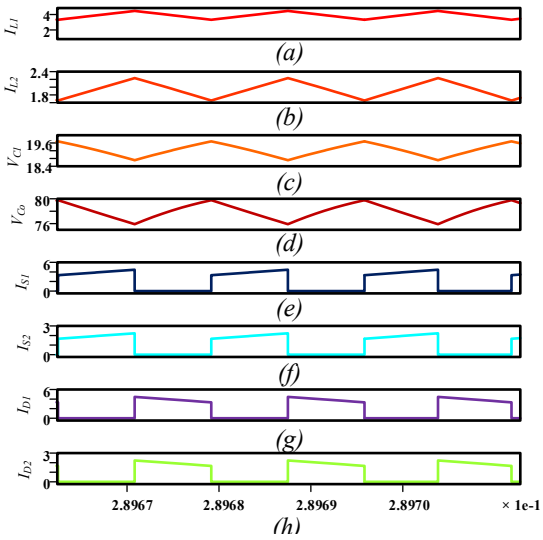

Fig. 7. Simulation results. (a) first inductor current, (b) the second inductor current, (c) the first capacitor voltage, (d) the output voltage.

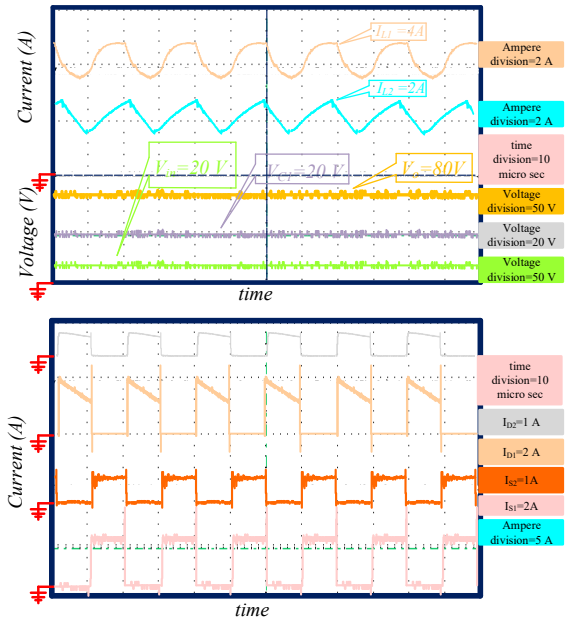

Fig. 8. Experimental results.

$$\begin{cases} V_{in}=20V \\ V_{c1}=20V \\ \mathrm{V_o}=80V \\ \Delta v_c=5\% \\ D=50\% \end{cases} \begin{cases} I_{L1}=4A \\ I_{L2}=2A \\ I_O=1A \\ \Delta i_L=30\% \\ \mathrm{f_s}=60\,\mathrm{kHz} \end{cases} \quad (22)$$

As can be understood, the output power has been assumed to be 80 W. By accounting for the assumed amount of the capacitor's voltage, the inductors' current, the capacitors' voltage ripple, the inductors' current ripple, and the value of the duty cycle and employing the theoretical relations of the inductors' current ripple and the capacitors' voltage ripple, the value of the inductors and the capacitors can be expressed.

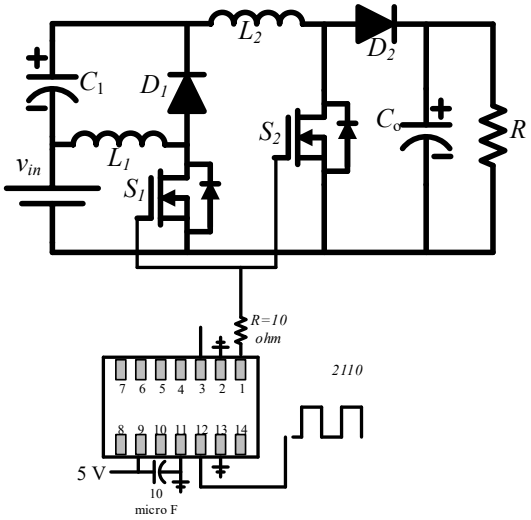

Fig.9. The explanation of the MOSFET driver

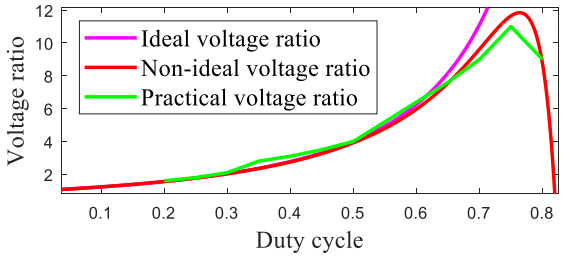

Fig. 10. The comparison of the ideal/non-ideal and practical voltage gains.

and the capacitors can be expressed. The mentioned values are as followed:

$$\begin{cases} L=140\mu H \\ L2=555\mu H \\ C_1=27\mu F \\ C_O=2.1\mu F \end{cases} \quad (23)$$

Fig. 7 refers to the simulation results. The inductors' average current and capacitors' average voltage are as (24), according to the simulation results:

$$\begin{cases} V_{c1}=19.6V \\ \mathrm{V_o}=78V \\ I_{L1}=4A \\ I_{L2}=2A \end{cases} \quad (24)$$

Comparing the extracted results and calculted results concludes their compatibilty. The negligible difference between the reported values stands from applying the parasitic components to the simulation setup. The experimental results of the designed topology have been extracted and illustrated in Fig. 8 to show the compatibility of the theoretical relations and simulation results with reality. It is good to note that IRF540 has been considered for the switches, FES8GT for the diodes, E-I type (45*35*15) inductor cores, and electrolyte and MKT capacitors in the prototype. It is worth noting that the mentioned assumptions in the simulation have been accounted in the experimental results.

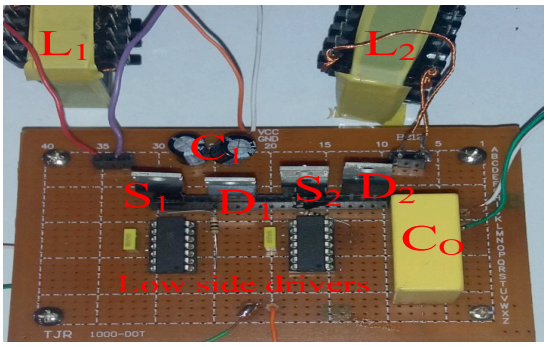

Fig. 11. The built-up circuit.

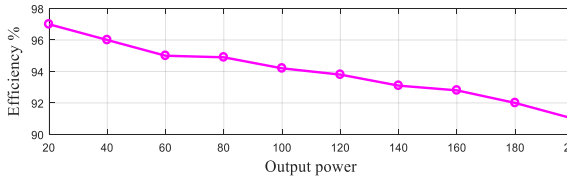

Fig. 12. The efficiency of the converter for the different output powers.

It is good to note that the calculated values in (23) are the minimum value of the components to satisfy the ripple considerations. Therefore, the capacitors have been considered as 100 and 10 micro F. Fig. 11 presents the prototype. It is good to note that IRF2110 is the MOSFET driver of the prototype, according to Fig. 9. Fig. 8 shows the voltage waveform of the input sources and capacitors. Moreover, the inductors' and semiconductors' current waveforms are the other extracted waveforms. The compatibility of the simulation results with the experimental outcomes proves the correctness of the extracted relations. Moreover, in Fig. 10, the practical voltage ratio has been extracted concerning the different amounts of the duty cycle. As can be understood, the non-ideal voltage ratio based on the extracted relation of the non-ideal voltage ratio is compatible with the practical voltage ratio based on the experimental outcomes. Moreover, the maximum value of the voltage ratio is 12 by 78 percent, according to the relation of the non-ideal voltage ratio. The practical results predicted the mentioned value of 11.8 by 75 percent as a value of the duty cycle. Fig. 12 illustrates the efficiency of the designed topology for the different output power values. The efficiency value based on the experimental results decreases from 97% to 91%, while the output power varies from 20W to 200W. Consequently, the expressed relations of the non-ideal voltage ratio are compatible with the experimental results. Therefore, the correctness of the theoretical relations is deduced.

8. Conclusion

This article proposed a modified form of the traditional step-up topology. The voltage gain was the quadratic form of the voltage gain of the traditional step-up topology. The continuity of the input current was kept, and the voltage/current stress of the semiconductor devices was low valued and suitable. The non-ideal mode of the designed topology was discussed, and the describing voltage gain of the mentioned model was extracted and compared with the practical voltage gain based on the experimental results. Moreover, the non-ideal voltage gain of the designed converter was compared with the non-ideal voltage gain of the high gain converters, and the capability of the designed converter was concluded. Moreover, the efficiency of the designed topology was discussed for 80 W of the output power. As the duty cycle becomes 50 %, the efficiency of the designed converter based on the experimental results was 95 %. The efficiency of the presented topology was discussed for different values of the output power for all amounts of the duty cycle. Furthermore, the various kinds of power loss were discussed for a duty cycle value, which concludes the voltage gain of 4 for the presented topology and other high gain converters, and the lower power loss of the designed converter was concluded. The small-signal analysis of the designed topology was discussed, and the bode diagram was extracted. The simulation outcomes based on PLECS software and the experimental results were extracted, compared, and their compatibility proved the correctness of all theoretical relations. These kinds of converters can be used HID lamps which require high voltage and low current. Moreover, such a DC-DC converter can be employed in electrical bicycles. Furthermore, the mentioned types of converters can be applied to micro inverters.

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