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An Improved Quadratic Boost Converter Suitable for Photovoltaic Applications

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ABSTRACT

Non-isolated DC–DC converters offer an effective solution to the limitations of isolated counterparts. This study proposes a new non-isolated DC–DC converter that integrates a conventional boost converter with a diode–capacitor voltage multiplier cell (VMC). The higher voltage gain is achieved without increasing the number of inductors, which remains the same as in Cuk, SEPIC, and Zeta converters. Similar to boost, Cuk, and SEPIC converters, the proposed topology ensures continuous input current and subjects the input filter capacitor to low current stress. It also provides a common ground between the load and source while maintaining positive output polarity. In addition to delivering a high voltage gain, the converter achieves low and acceptable voltage/current stresses on the semiconductors. Both ideal and non-ideal operating modes are analyzed. Finally, experimental results are presented to validate the theoretical analysis, with a 200 W prototype designed for 40 V input and 400 V output.

1. Introduction

The output voltage of photovoltaic (PV) panels is generally insufficient to directly supply a three-phase inverter for grid injection. Therefore, a DC-DC converter is required to step up the voltage level. As illustrated in Fig. 1, DC-DC converters are classified into isolated and non-isolated types. In isolated converters, the voltage gain primarily depends on the transformer turns ratio [1], which eliminates the need for high duty cycles. Despite this advantage, several drawbacks pose significant challenges. The use of a transformer increases both the volume and weight of the converter, thereby reducing power density [2]. In addition, the input current is discontinuous, which elevates the current stress on the input filter capacitor and consequently demands larger capacitance and size [3]. Furthermore, the current discontinuity imposes higher voltage stress on the switch, necessitating the use of snubber circuits that add complexity and cost [4]. These limitations collectively motivate the adoption of non-isolated DC-DC converters as a more practical alternative [5].

The boost converter is the most widely used non-isolated DC-DC converter with step-up capability [6]. It offers continuous input current and maintains a common ground between the source and the load [7]. However, despite these advantages, the boost converter has notable limitations. The voltage stress on its semiconductors is equal to the output voltage, which becomes a significant challenge at higher voltage levels [8]. In addition, achieving very high voltage gains is difficult [9]. Increasing the duty cycle to enhance voltage gain results in reduced efficiency. Therefore, improved non-isolated DC-DC converter topologies are needed to overcome these shortcomings [10].

The topologies proposed in [11]–[31] represent various improved non-isolated DC-DC converters. Among them, the converters in [11]–[15] are simple quadratic DC-DC converters, where the overall voltage gain is the product of the voltage gains of their sub-converters. Although these topologies provide higher voltage gains than conventional converters, their performance remains insufficient for photovoltaic (PV) applications. The converters presented in [16]–[19], [23], [24], and [28]–[31] combine quadratic DC-DC converters with voltage multiplier cells (VMCs) or voltage-lift techniques. These achieve higher voltage gains than the former group;

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however, they suffer from increased input current ripple, and the voltage stresses of the semiconductors remain close to the output voltage an issue more severe than in [11]–[15]. Additionally, the converters introduced in [20]–[22], [25]–[29] are improved versions of conventional non-isolated DC-DC

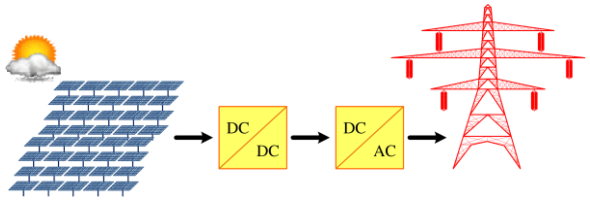

Fig. 1. Use of DC-DC converters I renewable applications.

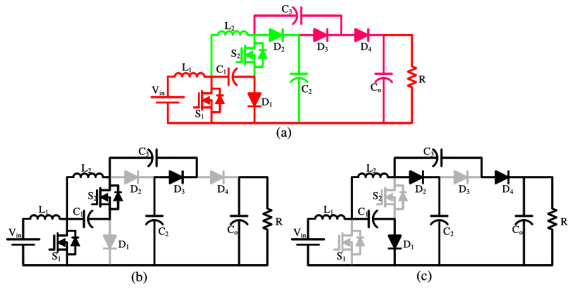

Fig. 2. (a) Proposed topology, (b) equivalent circuit of the first mode, (c) equivalent circuit of the second mode.

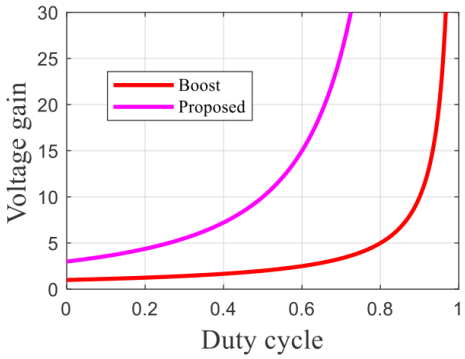

Fig. 3. Voltage gain comparison of the proposed topology and boost converter.

converters integrated with VMCs. While their voltage gain surpasses that of classic designs, they still cannot achieve a tenfold gain at low duty cycles. Furthermore, in [25], [27], and [29], the common ground between the input source and the load is eliminated, which limits their practical applicability.

This paper presents an improved quadratic boost topology that integrates a quadratic boost converter with a diode–capacitor voltage multiplier cell (VMC). The proposed design offers several key advantages, including continuous input current and a common ground between the load and the input source. Notably, the converter achieves high voltage gains even at low duty cycles. In addition, the voltage stress on the semiconductors remains significantly lower than the output voltage, ensuring improved reliability. Overall, the proposed topology provides a voltage gain that surpasses that of a simple cascade connection of its substructures.

2. The proposed Topology in the ideal mode

Fig. 2(a) illustrates the proposed converter topology, which integrates two boost stages with a diode–capacitor voltage multiplier cell (VMC). Incorporating the initial boost stage ensures continuous input current. Similar to the conventional boost converter, the proposed topology maintains a common ground between the load and the input source. The converter operates in two modes under ideal conditions and continuous conduction mode (CCM). Fig. 2(b) shows the equivalent circuit for the first operating mode, in which both switches and the third diode are ON. During this mode, the applied voltage magnetizes the inductors, and the activation of the third diode connects the series combination of the first and second capacitors in parallel with the third capacitor. The equivalent circuit of the second mode is shown in Fig. 2(c). Here, the applied voltage across the inductors is negative, causing demagnetization, while the series combination of the second and third capacitors becomes parallel with the output capacitor. Based on these operating principles, the steady-state inductor voltages and capacitor currents are as follows:

$$\begin{cases} V_{L1} = D(V_{in}) + (1-D)(V_{in} - V_{C1}) \\ V_{L2} = D(V_{C1}) + (1-D)(V_{C1} - V_o) \\ i_{C1} = D(-i_{L2} - i_2) + (1-D)(i_{L1} - i_{L2}) \\ i_{C2} = D(-i_2) + (1-D)(i_{L2} - i_3) \\ i_{C3} = D(i_2) + (1-D)(-i_3) \\ i_{Co} = D(-I_o) + (1-D)(i_3 - I_o) \end{cases} \quad (1)$$

By applying the voltage-second balance to the inductor voltage equations, the average inductor voltages can be expressed as follows:

$$\begin{cases} V_{C1} = \dfrac{V_{in}}{1-D} \\ V_{C2} = \dfrac{V_{in}}{(1-D)^2} \\ V_{C3} = \dfrac{2-D}{(1-D)^2} V_{in} \\ V_o = \dfrac{3-D}{(1-D)^2} V_{in} \end{cases} \quad (2)$$

By applying the current-second balance to the capacitor current equations, the average capacitor currents can be expressed as follows:

$$\begin{cases} I_{L1} = \dfrac{3-D}{(1-D)^2} I_o \\ I_{L2} = \dfrac{2}{1-D} I_o \\ i_2 = \dfrac{I_o}{D} \\ i_3 = \dfrac{I_o}{1-D} \end{cases} \quad (3)$$

In the previous equation, i2 and i3 represent inrush currents generated by the parallel connection of the capacitors. The extracted results show that the output voltage is higher than that of the conventional boost converter. Fig. 3 compares the voltage gain of the boost and proposed topologies. As shown, the proposed topology achieves a higher voltage gain than the boost converter across all duty cycles. Notably, it can provide a tenfold voltage gain at a 50% duty cycle.

By defining the average capacitor voltages and inductor currents, the voltage and current stresses of the semiconductors can be determined as follows:

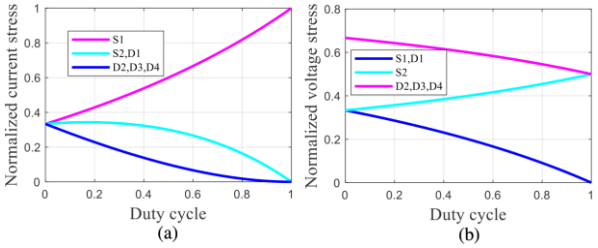

Fig. 4. (a) Normalized current stress of the semiconductors, (b) normalized voltage stress of the semiconductors.

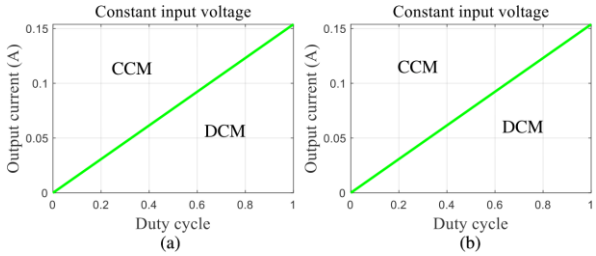

Fig. 5. Operating region of the converter between CCM and DCM according to the output current value and duty cycle, while: (a) input voltage is constant, (b) input voltage is constant.

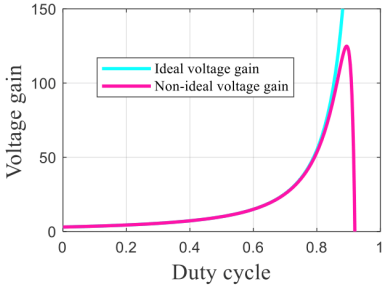

Fig. 6. Ideal and non-ideal voltage gains comparison of the proposed topology.

$$\begin{cases} I_{S1} = \dfrac{1+D}{(1-D)^2} I_o \\ I_{S2} = I_{D1} = \dfrac{1+D}{1-D} I_o \\ I_{D2,3,4} = I_o \end{cases} \quad (4)$$

$$\begin{cases} V_{S1} = V_{D1} = \dfrac{V_{in}}{1-D} \\ V_{S2} = \dfrac{V_{in}}{(1-D)^2} \\ V_{D2,3,4} = \dfrac{2-D}{(1-D)^2} V_{in} \end{cases} \quad (5)$$

Comparing the semiconductor current stresses with the input current shows that all current stresses are lower than the input current. Similarly, all voltage stresses are below the output voltage. By taking the output voltage as the voltage base and the input current as the current base, the normalized voltage and current stresses are shown in Fig. 4. As illustrated, all normalized stresses remain below unity, indicating that the semiconductors operate within acceptable limits.

The simplified expressions for the inductor current ripple and capacitor voltage ripple are given as follows:

$$\begin{cases} \Delta i_{L1} = \dfrac{DV_{in}}{L_1 f_s} \\ \Delta i_{L2} = \dfrac{DV_{in}}{(1-D)L_2 f_s} \end{cases} \quad (6)$$

$$\begin{cases} \Delta v_{c1} = \dfrac{(1+D)I_o}{(1-D)C_1 f_s} \\ \Delta v_{c2} = \dfrac{I_o}{C_2 f_s} \\ \Delta v_{c3} = \dfrac{I_o}{C_3 f_s} \\ \Delta v_{co} = \dfrac{DI_o}{C_o f_s} \end{cases} \quad (7)$$

The inductor values determine the magnitude of the current ripple. Notably, the inductor current ripple should not exceed twice the average inductor current. In other words, the minimum inductor value required to maintain continuous conduction mode (CCM) can be determined from:

$$\begin{cases} L_1 > \dfrac{D(1-D)^4 R}{2(3-D)^2 f_s} \\ L_2 > \dfrac{D(1-D)^2 R}{2(3-D) f_s} \end{cases} \quad (8)$$

Notably, the average inductor current also influences the transition between continuous and discontinuous conduction modes. If the average inductor current falls below half of the inductor current ripple, the converter enters discontinuous conduction mode (DCM). The inductor current depends on both the duty cycle and the average output current. Fig. 5 illustrates the converter's operating region between CCM and DCM as a function of the average output current and duty cycle. The equations used to generate these plots are as follows:

$$\begin{cases} I_o = \dfrac{V_o}{4 f_s L_2} \dfrac{D(1-D)^2}{3-D} \\ I_o = \dfrac{V_{in}}{4 f_s L_2} D \end{cases} \quad (9)$$

3. The proposed topology in the non-ideal mode

The voltage gain derived in Section II cannot fully describe the converter's behavior under all operating conditions. Therefore, the equivalent series resistances of the inductors (rL), switches (rS), and diodes (rD), along with the load resistance (R), are considered in the voltage gain calculation. Based on these considerations, the non-ideal voltage gain of the proposed topology is expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{3-D}{(1-D)^2} - \frac{r_L}{R}\frac{(3-D)^2}{(1-D)^6} - \frac{r_S}{R}\frac{D(3-D)^2}{(1-D)^6} - \frac{r_D}{R}\frac{(3-D)^2}{(1-D)^5} \quad (10)$$

Fig. 6 compares the ideal and non-ideal voltage gains of the proposed converter. As shown, the ideal and non-ideal gains do not match across all duty cycles, and the degree of agreement depends on the load value and the quality of the components. Fig. 7 illustrates the voltage gain behavior under variations in output power and component quality. From this figure, it is evident that changes in the

output power have the most significant impact on the voltage gain.

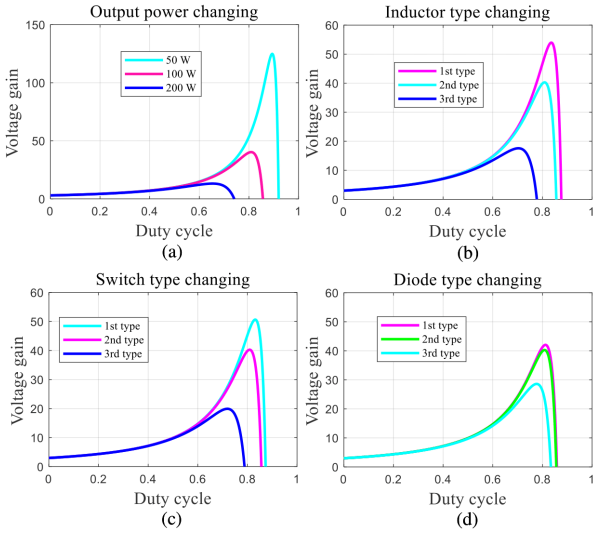

Fig. 7. Behavior of the non-ideal voltage gain according to the change of: (a) output power, (b) inductors type, (c) switches type, (d) diodes type.

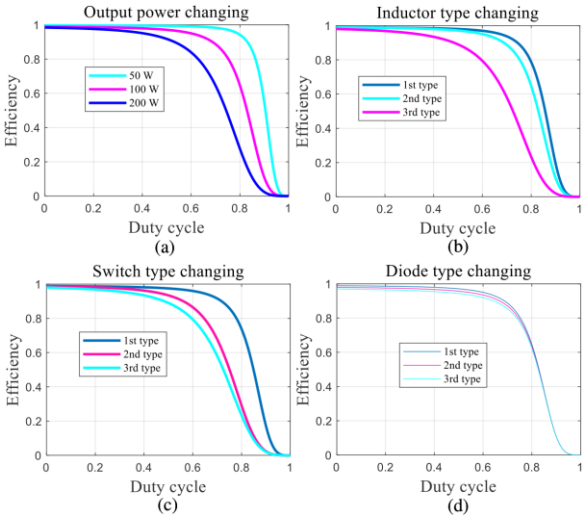

Fig. 8. Behavior of the efficiency according to the change of: (a) output power, (b) inductors type, (c) switches type, (d) diodes type.

The efficiency of the converter can be accurately determined based on its losses. In this study, only the conduction losses of the switches, inductors, and diodes are considered, while the switching and frequency-dependent losses are neglected. The mathematical expressions for these losses and the resulting efficiency are given as follows:

$$\begin{cases} P_L = \dfrac{2D^2-8D+10}{(1-D)^4}\dfrac{r_L}{R}P_o, P_{SC} = \dfrac{D^4-D^2+2D+2}{D(1-D)^4}\dfrac{r_S}{R}P_o \\ P_D = \dfrac{4-2D}{1-D}V_{DF}I_o, \eta = \dfrac{P_o}{P_o+P_L+P_{SC}+P_D} \end{cases} \quad (11)$$

The presented equations describe the converter's efficiency as a function of output power, component quality, and duty cycle. Figure 8 illustrates the efficiency variation with changes in output power and component quality. As shown, variations in output power have the most significant impact at higher duty cycles, whereas changes in diode type affect efficiency most at lower duty cycles.

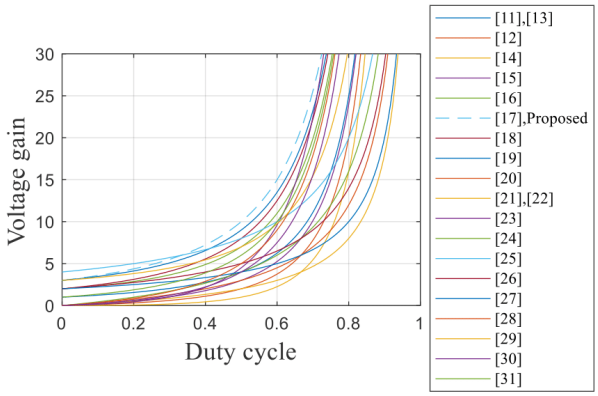

Fig. 9. Voltage gain comparison of the proposed topology with recently suggested converters.

4. Comparison of the proposed topology with other improved topologies

The proposed topology in this study is capable of providing a 10 times voltage gain at a 50% duty cycle, making it highly suitable for renewable energy applications. To illustrate its performance relative to recently suggested topologies, Fig. 9 presents a comparison of the voltage gain between the proposed converter and those in [11]–[31]. The superiority of the proposed topology is evident from this comparison. The number of components for each topology is summarized in Table I.

According to Table I, the number of inductors in the proposed topology matches that of [11], [13], [25], and [31]; it is fewer than in [12], [19], [24], [26], and [28]; and slightly more than in [27]. The number of capacitors in the proposed converter is equal to that in [17], [21], [25], [26], and [28]; fewer than in [24]; and greater than the rest. Regarding switches, the proposed topology uses the same number as in [11]–[15] and [28]–[31].

Additionally, the number of diodes in the proposed topology is fewer than in [16]–[19] and [23]–[25]. To provide a more comprehensive view of component utilization relative to voltage gain, the voltage gain density has been calculated and presented in Table II. This table integrates the information from Table I and Fig. 9. As shown, the voltage gain density per inductor is the highest, followed by that per diode, and then per all components. For capacitors, the voltage gain density in the proposed topology exceeds that of [12], [14], [15], and [20]–[24], but is lower than the remaining topologies. This analysis demonstrates that the proposed converter achieves high voltage gain with optimal component utilization.

Table III presents the voltage stress of the nearest switch and diode relative to the output voltage. In the proposed topology, the maximum voltage stress of all semiconductors remains below the output voltage, similar to [16], [17], [19], [20], [25], and [27]. In contrast, for the remaining converters, the semiconductor voltage stress equals or even exceeds the output voltage. This confirms the favourable operating conditions of the semiconductors in the proposed topology.

According to the efficiency, the reported references have discussed various topologies with various range of efficiency. Among these studies, the reported topology in [11] has report the efficiency of 95% to 97% in the operating point. In [13], [14], and [18], the efficiency

Table I. Components number

	L	C	S	D	All		L	C	S	D	All
[11]	2	2	2	2	8	[22]	3	4	1	2	10
[12]	3	3	2	2	10	[23]	5	3	1	9	18
[13]	2	2	2	2	8	[24]	5	5	1	7	18
[14]	3	3	2	2	10	[25]	2	4	1	5	12
[15]	3	3	2	2	10	[26]	3	4	1	4	12
[16]	3	3	1	7	14	[27]	1	3	1	3	8
[17]	3	4	1	6	14	[28]	3	4	2	3	12
[18]	3	3	1	5	12	[29]	2	3	2	3	10
[19]	3	4	1	5	13	[30]	2	3	2	3	10
[20]	3	6	1	3	13	[31]	2	3	2	3	10
[21]	3	4	1	2	10	[Proposed]	2	4	2	4	12

Table II. Gain density comparison

	G/L	G/C	G/S	G/D	G/All		G/L	G/C	G/S	G/D	G/All
[11]	2	2	2	2	0.5	[22]	0.66	0.5	2	1	0.2
[12]	0.66	0.66	1	1	0.2	[23]	0.9	1.5	4.5	0.5	0.25
[13]	2	2	2	2	0.5	[24]	1.6	1.6	8	1.14	0.44
[14]	0.33	0.33	0.5	0.5	0.1	[25]	4	2	8	1.6	0.66
[15]	1	1	1.5	1.5	0.3	[26]	1.66	1.25	5	1.25	0.41
[16]	2.33	2.33	7	1	0.5	[27]	4	1.33	4	1.33	0.5
[17]	3.33	2.5	10	1.66	0.71	[28]	1.66	1.25	2.5	1.66	0.41
[18]	2.66	2.66	8	1.6	0.66	[29]	3.5	2.33	3.5	2.33	0.7
[19]	3	2.25	9	1.8	0.69	[30]	2	1.33	2	1.33	0.4
[20]	1	0.5	3	1	0.23	[31]	3	2	3	2	0.6
[21]	0.66	0.5	2	1	0.2	[Proposed]	5	2	5	2.5	0.83

Table III. Semiconductors highest voltage stresses

	V_o	V_{S0}	V_{D0}		V_o	V_{S0}	V_{D0}
[11]	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	[22]	$\frac{3D}{(1-D)}V_{in}$	$\frac{V_{in}}{(1-D)}$	$\frac{V_{in}}{(1-D)}V_{in}$
[12]	$\frac{D}{(1-D)^2}V_{in}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	[23]	$\frac{D(1+D)^2}{(1-D)^2}V_{in}$	$\frac{(1+D)^2}{(1-D)^2}V_{in}$	$\frac{(1+D)^2}{(1-D)^2}V_{in}$
[13]	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	[24]	$\frac{4D}{(1-D)^2}V_{in}$	$\frac{4}{(1-D)^2}V_{in}$	$\frac{4}{(1-D)^2}V_{in}$
[14]	$\frac{D^2}{(1-D)^2}V_{in}$	$\frac{D}{(1-D)^2}V_{in}$	$\frac{D}{(1-D)^2}V_{in}$	[25]	$\frac{4}{(1-D)}V_{in}$	$\frac{2}{(1-D)}V_{in}$	$\frac{2}{(1-D)}V_{in}$
[15]	$\frac{2(2-D)}{(1-D)^2}V_{in}$	$\frac{D}{(1-D)^2}V_{in}$	$\frac{2-D}{(1-D)^2}V_{in}$	[26]	$\frac{2+D}{(1-D)}V_{in}$	$\frac{1+2D}{(1-D)}V_{in}$	$\frac{1+2D}{(1-D)}V_{in}$
[16]	$(1-\frac{1+D}{(1-D)^2})V_{in}$	$\frac{1+D}{(1-D)^2}V_{in}$	$\frac{1+D}{(1-D)^2}V_{in}$	[27]	$\frac{2}{(1-D)}V_{in}$	$\frac{1}{(1-D)}V_{in}$	$\frac{1}{(1-D)}V_{in}$
[17]	$\frac{3-D}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$	[28]	$\frac{D(3-D)}{(1-D)^2}V_{in}$	$\frac{(3-D)}{(1-D)^2}V_{in}$	$\frac{(3-D)}{(1-D)^2}V_{in}$
[18]	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$	[29]	$\frac{3-3D+D^2}{(1-D)^2}V_{in}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$
[19]	$(1-\frac{2}{(1-D)^2})V_{in}$	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$	[30]	$\frac{2D}{(1-D)^2}V_{in}$	$\frac{1+D}{(1-D)^2}V_{in}$	$\frac{1+D}{(1-D)^2}V_{in}$
[20]	$\frac{3D}{(1-D)}V_{in}$	$\frac{V_{in}}{(1-D)}$	$\frac{V_{in}}{(1-D)}V_{in}$	[31]	$\frac{1+D}{(1-D)^2}V_{in}$	$\frac{1+D}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$
[21]	$\frac{2D}{(1-D)}V_{in}$	$\frac{V_{in}}{(1-D)}$	$\frac{V_{in}}{(1-D)}V_{in}$	[Proposed]	$\frac{3-D}{(1-D)^2}V_{in}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{2-D}{(1-D)^2}V_{in}$

varies between 91% to 94%. In [16] and [17] the efficiency changes from 94% to 96%. Additionally, in [20] and [22], the reported efficiency is from 96% to 97%. Finally, the presented topology in [30] has an efficiency from 94% to 95%. The rest of the converters in the reference do not achieve the desired and high efficiency. In the case of the proposed topology, the efficiency is more than 95% at the operating point.

5. Possible extensions of the proposed topology

The proposed topology is capable of providing other extensions besides keeping the advantages of the proposed topology and solving its disadvantages. In the second section, it was discussed that the voltage stress challenge of the semiconductors is solved. However, the output voltage is applied to a single capacitor at the output terminal. Therefore, it must be considered in output voltage selection. In Fig. 10, the first extension of the proposed topology is presented to solve the voltage stress challenge of the output terminal capacitor. As shown in this figure, the second capacitor in the proposed topology has been stacked with the output voltage, and a stacked connection of two capacitors acts as the output terminal capacitors.

The stacked connection of the capacitors at the output provides the output voltage by the voltage summation of the two capacitors. Another advantage of this type of extension is the use of the previous stage capacitor's voltage at the output. This form of design leads to the effectiveness of the arrangement. This topological advantage takes place without changing the voltage gain or topological advantage of the proposed converter. Here, the voltage of the capacitors and the voltage/current stress of the semiconductors are as follows in this extension:

$$\begin{cases} V_{C1}=\dfrac{V_{in}}{1-D} \\ V_{C2}=\dfrac{2-D}{(1-D)^2}V_{in} \\ V_{C3}=\dfrac{2-D}{(1-D)^2}V_{in} \\ V_{C4}=\dfrac{V_{in}}{(1-D)^2} \\ V_o=V_{C3}+V_{C4} \\ V_o=\dfrac{3-D}{(1-D)^2}V_{in} \end{cases} \quad (12)$$

$$\begin{cases} V_{S1}=\dfrac{V_{in}}{1-D} \\ V_{S2}=\dfrac{V_{in}}{(1-D)^2} \\ V_{D1}=\dfrac{V_{in}}{1-D} \\ V_{D2}=\dfrac{2-D}{(1-D)^2}V_{in} \\ V_{D3}=\dfrac{2-D}{(1-D)^2}V_{in} \\ V_{D4}=\dfrac{2-D}{(1-D)^2}V_{in} \end{cases} \quad (13)$$

$$\begin{cases} I_{S1}=\dfrac{1+D}{(1-D)^2}I_o \\ I_{S2}=\dfrac{1+D}{1-D}I_o \\ I_{D1}=\dfrac{1+D}{1-D}I_o \\ I_{D2}=I_o \\ I_{D3}=I_o \\ I_{D4}=I_o \end{cases} \quad (14)$$

Fig. 11 shows the other extensions of the proposed topology. These extensions are created by using inductor-based voltage multiplier cells instead of the inductors in the proposed topology. If the use of only one multiplier cell instead of one of the inductors causes 4 other extensions. Using the first cell instead of the second inductor provides a voltage gain as follows:

$$\frac{V_o}{V_{in}}=\frac{5-D}{(1-D)^2} \quad (15)$$

Using the second cell instead of the second inductor leads to a voltage gain as follows:

$$\frac{V_o}{V_{in}}=\frac{3+D}{(1-D)^2} \quad (16)$$

Using the first cell instead of the first inductor leads to a voltage gain as follows:

$$\frac{V_o}{V_{in}}=\frac{6-2D}{(1-D)^2} \quad (17)$$

Using the second cell instead of the first inductor leads to a voltage gain as follows:

$$\frac{V_o}{V_{in}}=\frac{(3-D)(1+D)}{(1-D)^2} \quad (18)$$

Using both the cells instead of both the inductors causes four other extensions. Using the first cell instead of both the inductors leads to a voltage gain reported as below:

$$\frac{V_o}{V_{in}}=\frac{10-2D}{(1-D)^2} \quad (19)$$

Using the first cell instead of the first inductor and the second cell instead of the second inductor leads to a voltage gain, reported as below:

$$\frac{V_o}{V_{in}}=\frac{2(3+D)}{(1-D)^2} \quad (20)$$

Using the first cell instead of the second inductor and the first cell instead of the second inductor leads to a voltage gain, reported as below:

$$\frac{V_o}{V_{in}}=\frac{(5-D)(1+D)}{(1-D)^2} \quad (21)$$

Using the second cell instead of both the inductors leads to a voltage gain reported as below:

$$\frac{V_o}{V_{in}}=\frac{(3+D)(1+D)}{(1-D)^2} \quad (22)$$

It can be understood that the provided voltage gain by the second to ninth extensions is more than the voltage gain in the proposed topology and its first extension. This achievement is gained besides keeping other advantages of the proposed topology.

6. Application of the proposed topology

The output voltage of photovoltaic panels or other renewable energy sources is generally insufficient for feeding 3-phase inverters to generate AC voltage for grid connection. As illustrated in Fig. 12, a high step-up DC-DC converter is required in parallel with the renewable energy sources to boost their output voltage, making it compatible with the inverter input. The proposed converter achieves this high voltage gain with a relatively low duty cycle. For instance, the proposed topology can provide a 10-fold voltage increase at a 50% duty cycle, raising the output voltage of the panels to over 400 V.

7. Small signal analysis

In order to design a suitable controller of the proposed topology, state space matrices must be presented. It is good to note that the independent inductors' current and the independent capacitors' voltage are the state space variables. In the proposed topology, the inductors are independent. However, the capacitors are not. In other words, the employed capacitor-based voltage multiplier cell has dependent capacitors due to their parallel/series connection. According to this explanation, the state space matrices are as follows:

$$A=\begin{pmatrix} 0 & 0 & \frac{-(1-D)}{L_1} & 0 \\ 0 & 0 & \frac{3-D}{2L_2} & \frac{-(1-D)}{2L_2} \\ \frac{2(1-D)}{3C_1} & \frac{5D-9}{6C_1} & 0 & \frac{1}{RC_1} \\ 0 & \frac{1-D}{3C_o} & 0 & \frac{-1}{RC_o} \end{pmatrix},\ B=\begin{pmatrix} \frac{V_{c1}}{L_1} \\ \frac{V_o-V_{c1}}{2L_2} \\ \frac{-\frac{2}{3}I_{L1}+\frac{5}{6}I_{L2}}{C_1} \\ \frac{-I_{L2}}{2C_o} \end{pmatrix},\ C^t=\begin{pmatrix} 0 \\ 0 \\ 0 \\ 1 \end{pmatrix} \quad (23)$$

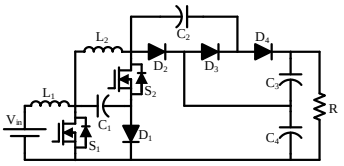

Fig. 10. The first extension of the proposed topology.

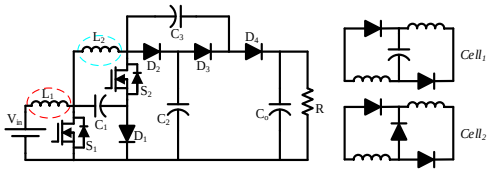

Fig. 11. The general way of the second to ninth extensions' creation.

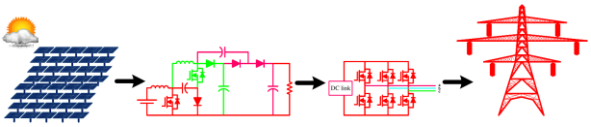

Fig. 12. Suitable application of the proposed topology.

According to these matrices, the Bode diagram of the proposed topology has been illustrated in Fig. 13(a) before the compensation. Using these equations in the sisotool of Matlab leads to the controller as below to provide the stability requirements.

$$C(s)=\frac{0.8}{s} \quad (24)$$

Applying this controller to the proposed topology leads to the Bode diagram of the converter for after compensation as Fig. 13(b). According to this figure, the phase and gain margins are positive, which indicates the stability of the converter.

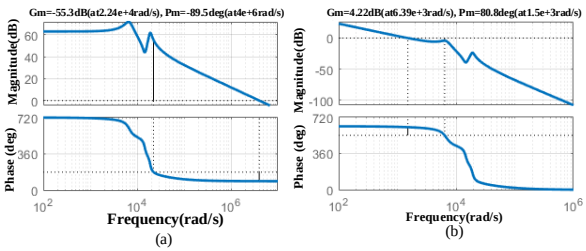

Fig. 13. Bode diagram of the proposed topology: (a) before compensation, (b) after compensation.

8. Experimental results

The theoretical analysis of the proposed topology was discussed in the previous section. In this section, the experimental results are presented to validate the theoretical predictions. The key design considerations for the converter include the input voltage, output current, switching frequency, inductor current ripple, and capacitor voltage ripple. The corresponding values, based on laboratory equipment constraints, are listed in Table IV. Using these values and the theoretical relations

presented in Section II, the average capacitor voltages, average currents of the inductors and semiconductors, and the peak voltages of the semiconductors are summarized in Table V. The switches used are IRF540, and the diodes are FXR16560F.

Figure 14 shows the prototype of the proposed topology. Figures 15 to 17 illustrate the experimental results, showing the voltage waveforms of the capacitors and semiconductors, as well as the current waveforms of the inductors and semiconductors. Comparing the average capacitor voltages and inductor/semiconductor currents, along with the peak semiconductor voltages, to the values reported in Table V demonstrates good agreement between experimental and theoretical results. Minor deviations are attributed to parasitic effects in the circuit components. Figure 18 presents the converter's efficiency across various output powers, with an output voltage of 400 V, a duty cycle of 50%, and an input voltage of 40 V. The results indicate that the converter maintains an efficiency above 90% over a wide range of output powers. In Figs. 19 and 20 discuss the behavior of the voltage gain and efficiency in relation to changes in output power and component quality. These figures show approximately the same behaviours in the third section for the voltage gain and efficiency. This compatibility validates the extracted relations. Moreover, the extracted values can be improved by the use of high-quality components.

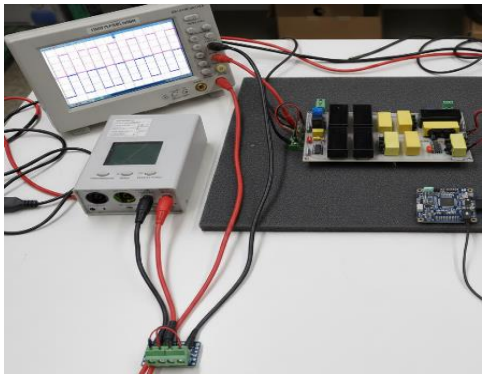

Fig. 14. Prototype of the proposed topology.

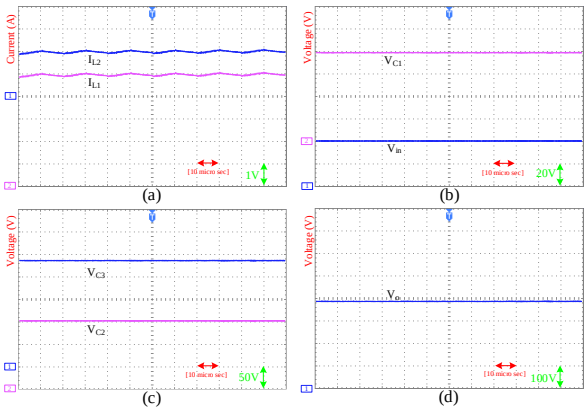

Fig. 15. Experimental results: (a) inductors' current, (b) voltage of input source and 1st capacitor, (c) voltage of the 2nd and 3rd capacitors, (d) voltage of the output capacitor.

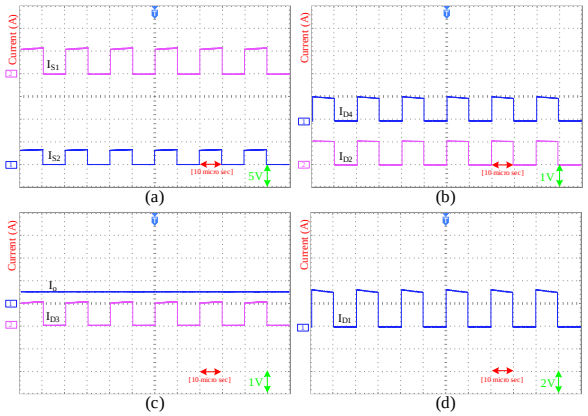

Fig. 16. Experimental results: (a) current of 1st and 2nd switches currents, (b) current of 2nd and 4th diodes, (c) output current and 3rd diode's current, (d) 1st diode's current.

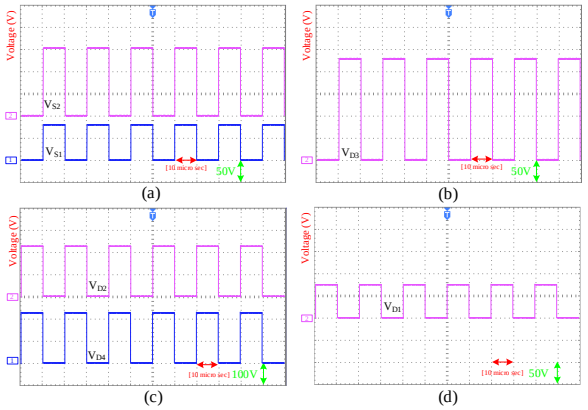

Fig. 17. Experimental results: (a) 1st and 2nd switch voltage, (b) 3rd diode voltage, (c) 2nd and 4th diode voltage, (d) 1st diode voltage.

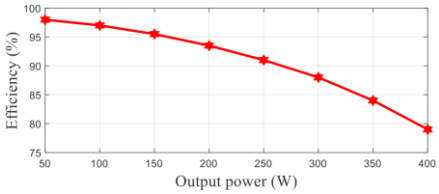

Fig. 18. Efficiency of the proposed topology according to the experimental results according to the change of the output power.

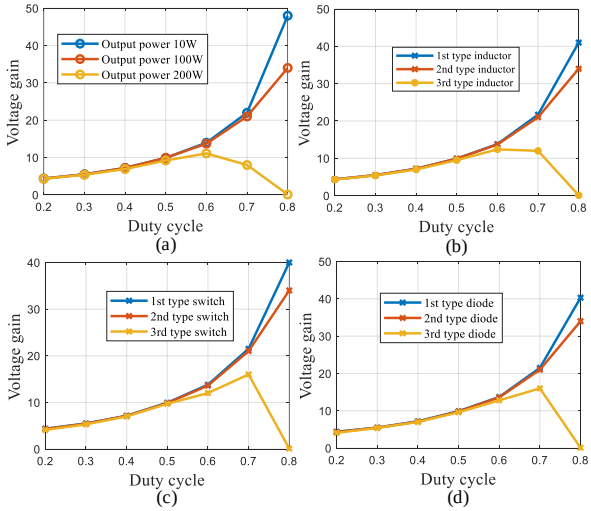

Fig. 19. Sensitivity analysis of the voltage gain according to the change of: (a) output power, (b) inductor type, (c) switch type, (d) diode type in experiment.

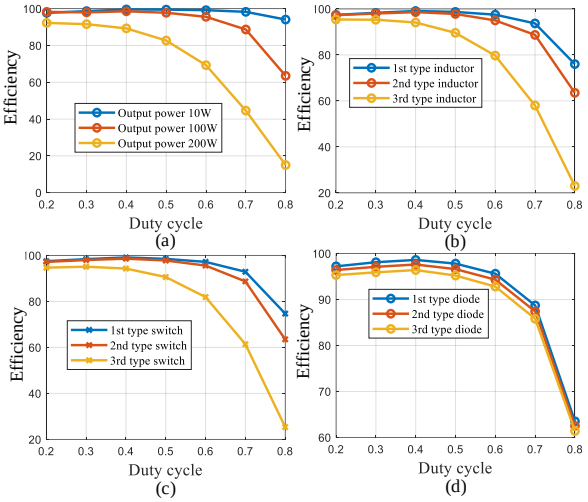

Fig. 20. Sensitivity analysis of the efficiency according to the change of: (a) output power, (b) inductor type, (c) switch type, (d) diode type in experiment.

Table IV. Design considerations

V_{in}	f_s	I_o	Δi_l	ΔV_c	D
40 V	50 kHz	0.5 A	30%	5%	50%

Table V. Predicted values by the theoretical relations

Parameter	Value	Parameter	Value
V_{C1}	80 V	I_{S1}	3 A
V_{C2}	160 V	$I_{S2} = I_{D1}$	1.5 A
V_{C3}	240 V	$I_{D2,3,4}$	0.5 A
V_{Co}	400 V	$V_{S1} = V_{D2}$	80 V
I_{L1}	5 A	V_{S2}	160 V
I_{L2}	2 A	$V_{D2,3,4}$	240 V

Table VI. Minimum value of the inductors and capacitors

L_1	L_2	C_1	C_2	C_3	C_o
0.25 mH	1.333 mH	7.5 µF	1.25 µF	0.83 µF	0.25 µF

9. Conclusion

In this paper, an improved quadratic boost topology is proposed and analyzed in both ideal and non-ideal operating modes. Experimental results are presented and compared with the theoretical predictions, demonstrating a strong agreement between them. Based on the findings, the proposed topology is shown to be well-suited for renewable energy applications.

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