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A Novel Asymmetrical Cross-Switched Cascaded Multilevel Inverter With Low Total Standing Voltage and Comparative Evaluation of Switching Strategies

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ABSTRACT

This paper analysis common switching patterns on a proposed converter. The converter is an asymmetrical multilevel inverter (MLI) based on cross switched cascaded. Multilevel inverters, as power electronic converters for converting direct current (DC) sources to alternative current (AC) forms, are become popular because of their advantages. Advantages such as high quality of voltage and power, low switching frequency, modularity and extendibility, and low electro-magnetic interference (EMI). MLIs usually have more components, especially switches. Low total stand voltage (TSV) of switches decreases the cost and losses of MLIs. The proposed cross switched cascaded multilevel inverter (CSCMLI) has low TSV and easy extendibility. The switching of MLIs is one of the most important parts of operation due to the noticeable number of switches. In this paper, some of the common switching techniques are mentioned, four of them are simulated, and finally, two of the most appropriate and the simplest are suggested and applied for earning low total harmonic distortion (THD) at the output voltage. The proposed MLI is analyzed at 21 output voltage levels (OVLs) and compared with recently published MLIs from different aspects. The proposed MLI, first, is simulated in MATLAB/SIMULINK, then for more validation, a sample is generated and experimented in the lab.

1. Introduction

As time passes, multilevel inverters (MLIs) have extended and become an effective technology in industry and power electronics due to their advantages. Low switching frequency and stress voltage on switches, low THD of output voltage and EMI, and extendibility and modularity are some of their advantages. MLIs, because of their expandability, are attractive converters for medium and high-voltage and power applications. These structures, by identified switching method, generate AC voltage from one or more DC sources like flying capacitors (FC), fuel cell (FUC), photovoltaics (PVs), and batteries. MLIs combine low-voltage (LV) DC sources to produce a stepped, waveform that is near sinusoidal, high voltage (HV). Increasing the number of output voltage levels (steps) decreases the THD of the output voltage and improves power quality. But this increment intensifies components of power electronics and DC voltage sources. Switches have a key role in MLIs. They are switched under various voltages, and the reduction of their voltage stress causes a decrease in price, losses, and, improvement in the lifetime of the converter and efficiency [1].

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1.1. Classification of Multilevel inverters

Multilevel inverters are generally classified into three basic groups. The first one is Cascaded H Bridge (CHB) MLI. Each module consists of a DC voltage source and four switches. This MLI can be extended by cascading several modules and producing more output voltage levels (OVLs). The second one is neutral point clamp (NPC). This one uses several diodes to be connected to a neutral point. The last one is flying capacitor (FC). This topology applies one DC source, but existence of a few capacitors increases the size and complexity of this MLI [2−4]. Multilevel inverters, according to the value of DC sources, are generally classified into two groups: symmetric and asymmetric. In symmetrical MLI, the values of DC voltage sources are identical, but in asymmetrical MLI, they have different quantities, and according to the sequence of DC voltage values, MLIs can generate different OVLs [2]. Multilevel inverters have different structures, and among them, those that can be cascaded, such as cascaded multilevel inverters (CMIs), like CHB, are more interesting because of their ability to develop and produce high output voltage levels [5, 6].

1.2. MLIs Applications

Multilevel inverters are broadly used in industry and power electronics applications like improvement devices of power quality such as Flexible Alternating Current Transmission Systems (FACTS), static compensators, high voltage direct current (HVDC), especially with the development of renewable energies, improvers of power quality, active filters, solid-state transformers, motor drives, and marine propulsion. In addition, multilevel inverters are utilized in PV systems and variable-frequency drives [7−12].

1.3. Main challenges of MLIs

The advantages and applications of MLIs are increasing their popularity, but the high number of components, especially in higher OVLs, is the main disadvantage of these converters. Decreasing the mentioned problem has led attention to the utilization of asymmetrical MLIs. This kind of MLI has different values of DC sources and can generate more OVLs. Various DC voltage sources cause different stress voltage on semiconductors, especially switches, and those that are near high voltage are under much stress. To overcome this issue, the MLIs should be designed with low TSV to improve the lifetime of switches and converters and decrease the losses and price of MLIs. Easy extendibility for connection of more DC sources and low THD of output voltage for applying small filters are other challenges of MLIs.

1.4. Review of presented converters

Reference [13] suggests a general structure for MLI. This structure operates in three various modes according to the value of DC sources. The converter includes two basic parts and one middle bridge. By adding more basic parts equally to the left and right of the middle part, more output voltage levels can be produced. But this MLI has a high TSV and more elements for development. In reference [14], an asymmetrical MLI based on capacitor switching and voltage-boosting capability has been presented. This MLI extends modularity, so more components are needed. Although capacitor-switching-based multilevel inverters reduce the number of voltage sources, current spikes can happen and damage elements through the source and capacitor. MLI of reference [14] suffers from high TSV and more components for development. Reference [15] presents a novel MLI with a reduced number of components. This converter consists of two parts. The first part produces voltage just at one pole, and the second part is an H Bridge (HB) for generating positive and negative voltage. The first part includes two DC voltage sources on two sides. This part can expand and generate more OVLs by increasing the number of capacitors and switches on each side equally. In this kind of multilevel inverter, four switches of the HB inverter endure the peak voltage of the converter, so the TSV of them is high. High TSV and the number of elements are the main disadvantages of reference [15]. Reference [16] presents a modular MLI that has 8 switches and 3 DC voltage sources. This structure, according to the value of DC sources, operates in three different modes. This converter is developed by a series connection of more modules. So, more components are needed in high OVLs. In references [17] and [18], new MLIs with a reduced number of components have been proposed. They include two parts. The first part, with extending possibilities, generates a voltage in one pole, and the second part is an HB inverter for generating positive and negative poles. The MLI of reference [17] works only asymmetrically and has two modes. But the converter in [18] has several modes according to various amounts of DC sources. High TSV and the number of components are the main disadvantages of [17] and [18]. The authors have suggested symmetric and asymmetric d-type MLI in reference [19]. This modular converter is developed by series connecting each module. So, more components are necessary at high levels. References [20] and [21] present novel MLIs with the Model Predictive Nearest Level Control (MP-NLC) switching technique. These converters have more components in comparison with the proposed structure, and implementation of this switching strategy is complicated. In reference [22], the authors present an MLI based on a series connection of sub-multilevel units with an H-bridge inverter at the end of each sub-multilevel for generating two poles. This converter suffers from high TSV. Reference [23] suggests a cascaded H-Bridge MLI with an adjustable DC-link and Selected Harmonic Mitigation (SHM) switching technique. In the mentioned switching strategy, finding optimal angles for mitigating defined harmonics is challenging. Reference [24] presents a novel asymmetrical MLI with a reduced number of components. In this topology with increment of sources the number of bidirectional switches increases correspondingly. Therefore, in high OVLs losses are considerable. Also, this structure has high TSV compared to the proposed one. Reference [25] uses a hysteresis switching control for producing AC output voltage from a multi-input solar converter. Although this strategy is done close-loop but high switching frequency is the main defect of this technique. In [26], a crisscross switched multilevel inverter (MLI) employing cascaded semi-half-bridge unit

with both symmetrical and asymmetrical modes has been introduced. This configuration requires a large number of DC sources and switches in order to generate high output voltage levels.

This paper investigates several switching strategies on the proposed asymmetrical multilevel inverter to overcome the mentioned weaknesses. The advantages of the proposed multilevel inverter are as follows:

- ***Low THD due to a simple and proper switching strategy***
- ***Noticeably low TSV***
- ***Proper efficiency and number of components***
- ***Simple expandability***
- ***No need for an H-Bridge inverter.***

2. Proposed Structure

This paper presents a novel multilevel inverter (MLI) topology that aims to retain the advantages of the existing topologies while mitigating their inherent drawbacks. One of the major limitations of the existing structures is the high voltage stress imposed on power semiconductor devices, particularly the switches. Since switches are among the most critical components in power electronic converters, reducing the total standing voltage (TSV) across all switches not only lowers the switch voltage rating and, consequently, the overall converter cost, but also reduces power losses and improves conversion efficiency. Furthermore, owing to the sinusoidal nature of the output voltage in MLIs, achieving a low total harmonic distortion (THD) is essential for minimizing the size and cost of the output filter. In addition, scalability is another key requirement that a multilevel inverter topology should satisfy.

To address the limitations of the aforementioned studies, a new converter topology derived from the structure presented in [29] is proposed. The inverter introduced in [29] employs a symmetric configuration and does not support asymmetric operation. Consequently, achieving a higher number of output voltage levels requires the use of additional DC sources and switching devices, which increases the overall converter complexity and cost.

The proposed topology adopts an asymmetric configuration, enabling the generation of a higher number of output voltage levels while utilizing a reduced number of power electronic components. In addition, the proposed converter exhibits proper scalability, as each added cell (unit) consists of only one DC source and two unidirectional switches. The control scheme and switching strategy play a crucial role in the performance of multilevel inverters. An effective switching strategy not only ensures a low total harmonic distortion (THD) in the output voltage but also minimizes switching losses, thereby improving the overall converter efficiency. Furthermore, compared with the other investigated topologies, the proposed converter achieves a lower total standing voltage (TSV), making it a more cost-effective and efficient solution.

Fig. 1. illustrates the proposed asymmetrical multilevel inverter. To transform the symmetric multilevel inverter presented in [29] into an asymmetric topology, an additional DC source with a magnitude of (V_1 = -V_{dc}) is required to generate all output voltage levels. The most appropriate location for incorporating this source is adjacent to the source (V_2 = V_{dc}). This converter is based on CSCMLI. The proposed MLI includes two parts: basic and developer. The basic part consists of two parts with two DC voltage sources and 10 switches (4 bidirectional and 2 single switches). The developer part consists of just one DC source and two switches. This feature makes it easy to extend the proposed MLI for higher voltage and power applications. The sources (V_1) and (V_2) must never be connected to the circuit simultaneously, as this would result in a short-circuit condition. Therefore, the switches associated with these two sources are implemented as bidirectional switches to ensure safe and reliable operation. This converter, due to the sequence of DC voltage sources, operates in two modes. In the below equations, $\boldsymbol{N_{IGBT}}$, $\boldsymbol{N_{GD}}$, and $\boldsymbol{N_{Level}}$ are the number of switches, gate driver circuits, and OVLs in order. p is the mark of each DC source, and n is the number of DC sources. $\boldsymbol{V_{dc}}$ is the value of each step of the output voltage and also the smallest voltage source.

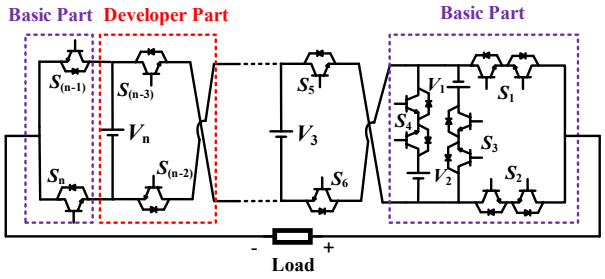


Fig. 1. The proposed MLI.

1- First mode

$$V_p=\begin{cases} V_{dc} & \text{If } p\leq 2 \\ (p-1)*V_{dc} & \text{If } p\geq 2 \\ p=1,2,\dots,n & \end{cases} \quad (1)$$

$$N_{Level}=\begin{cases} 3 & \text{If } n\leq 2 \\ n^2-n+1 & \text{If } n>2 \end{cases} \quad (2)$$

2- Second mode

$$V_p=\begin{cases} V_{dc} & \text{If } p\leq 2 \\ 3*2^{(p-3)}*V_{dc} & \text{If } p>2 \\ p=1,2,\dots,n & \end{cases} \quad (3)$$

$$N_{Level}=\begin{cases} 3 & \text{If } n\leq 2 \\ ((3\sum_{p=3}^{n}2^{(p-3)})+1)*2+1 & \text{If } n>2 \end{cases} \quad (4)$$

N_{IGBT}, N_{GD} and TSV are the same in two modes of 1 and 2 as follow:

$$N_{IGBT} = 2n+6 \quad (5)$$

(5)

$$N_{GD} = 2n+2 \quad (6)$$

(6)

$$TSV = 4\sum_{p=1}^{n} V_p \quad (7)$$

3. Analysis and comparison

The number of OVLs completely affects TSV, the number of switches, and sources. A sample of 21 OVLs is considered and investigated. This sample is from mode 2 and has four DC sources. Other parameters can be obtained from equations of (3)-(7). Fig. 2 depicts the proposed MLI in 21 output voltage levels and some of it's modes. In addition, Table I shows the situation of 10 switches in the MLI of 21 OVLs and number of conducted switches at each level. The proposed topology requires only four bidirectional switches to generate any number of OVLs, and the number of bidirectional switches remains unchanged even when the proposed topology is extended. As shown in Table I, only one or two of the bidirectional switches conduct at each OVL. Therefore, the converter losses do not increase significantly due to the use of bidirectional switches.

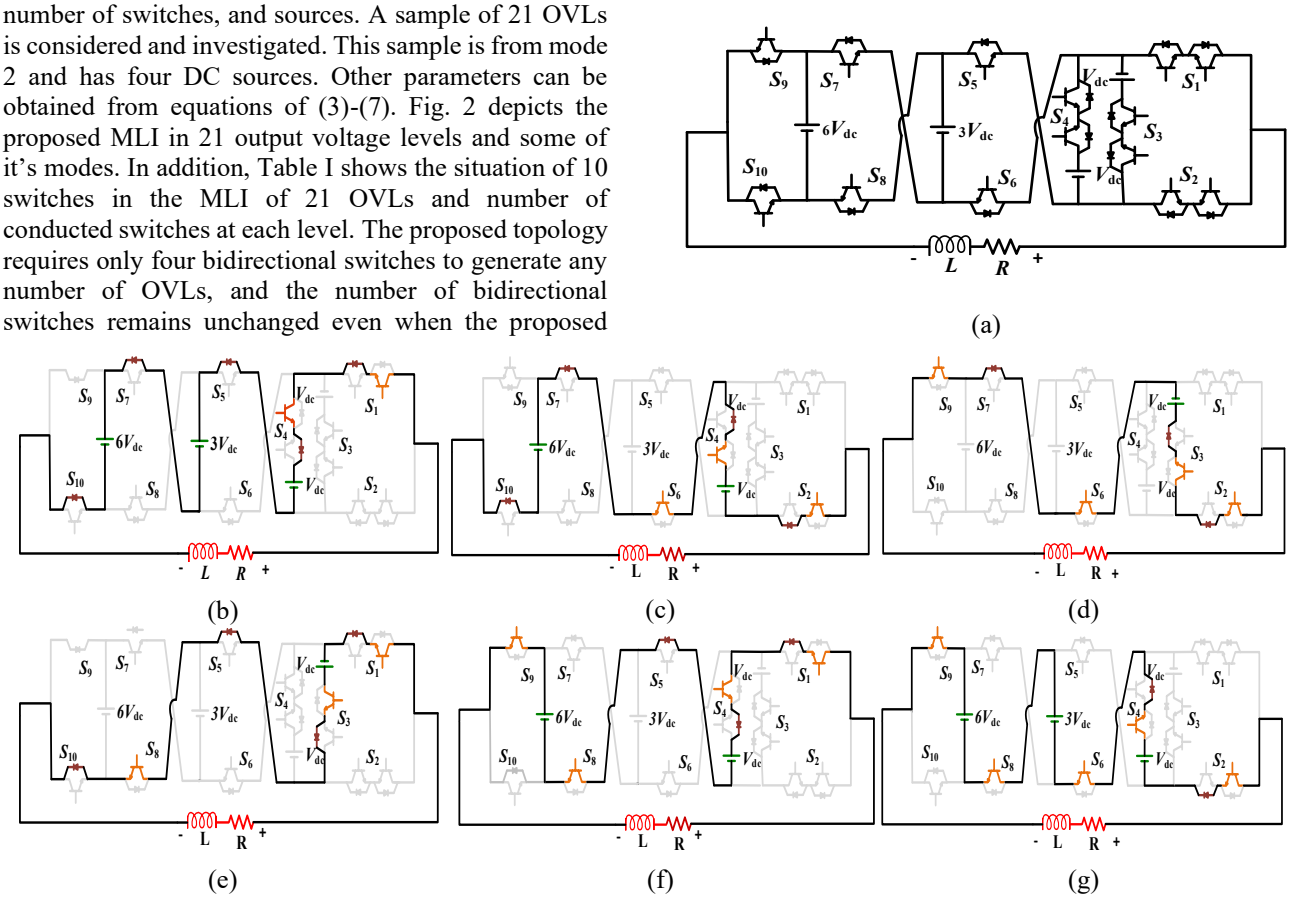


Fig. 2. The proposed MLI at 21 OVLs and some of the modes. (a) The general structure of 21 OVLs, (b) +10 level, (c) +5 level, (d) +1 level, (e) -10 level, (f) -5 level, (g) -1 level.

TABLE I. SWITCHING SITUATION OF S_1 TO S_{10} OF THE PROPOSED MLI IN 21-LEVEL AND NUMBER OF CONDUCTED SWITCHES.

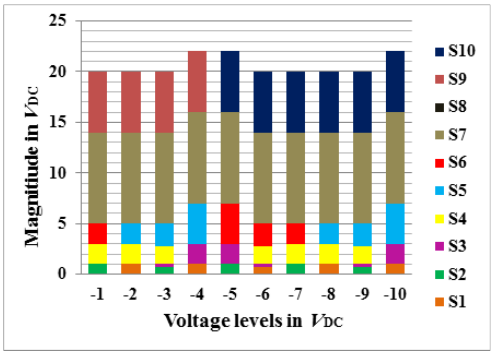
V_{Load}	Remark	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	Number of conducted bidirectional switches	Number of conducted switches
$10V_{dc}$	$V_4+V_3+V_2$	1	0	0	1	1	0	1	0	0	1	**2 out of 4**	**5 out of 10**
$9V_{dc}$	V_4+V_3	0	1	0	0	1	0	1	0	0	1	**1 out of 4**	**4 out of 10**
$8V_{dc}$	$V_4+V_3-V_1$	1	0	1	0	1	0	1	0	0	1	**2 out of 4**	**5 out of 10**
$7V_{dc}$	V_4+V_1	0	1	1	0	0	1	1	0	0	1	**2 out of 4**	**5 out of 10**
$6V_{dc}$	V_4	1	0	0	0	0	1	1	0	0	1	**1 out of 4**	**4 out of 10**
$5V_{dc}$	V_4-V_2	0	1	0	1	0	1	1	0	0	1	**2 out of 4**	**5 out of 10**
$4V_{dc}$	V_2+V_3	1	0	0	1	1	0	1	0	1	0	**2 out of 4**	**5 out of 10**
$3V_{dc}$	V_3	0	1	0	0	1	0	1	0	1	0	**1 out of 4**	**4 out of 10**
$2V_{dc}$	V_3-V_1	1	0	1	0	1	0	1	0	1	0	**2 out of 4**	**5 out of 10**
V_{dc}	V_1	0	1	1	0	0	1	1	0	1	0	**2 out of 4**	**5 out of 10**
0	**0**	1	0	0	0	0	1	1	0	1	0	**1 out of 4**	**4 out of 10**
$-V_{dc}$	$-V_1$	1	0	1	0	1	0	0	1	0	1	**2 out of 4**	**5 out of 10**
$-2V_{dc}$	V_1-V_3	0	1	1	0	0	1	0	1	0	1	**2 out of 4**	**5 out of 10**
$-3V_{dc}$	$-V_3$	1	0	0	0	0	1	0	1	0	1	**1 out of 4**	**4 out of 10**
$-4V_{dc}$	$-V_2-V_3$	0	1	0	1	0	1	0	1	0	1	**2 out of 4**	**5 out of 10**
$-5V_{dc}$	V_2-V_4	1	0	0	1	1	0	0	1	1	0	**2 out of 4**	**5 out of 10**
$-6V_{dc}$	$-V_4$	0	1	0	0	1	0	0	1	1	0	**1 out of 4**	**4 out of 10**
$-7V_{dc}$	$-V_4-V_1$	1	0	1	0	1	0	0	1	1	0	**2 out of 4**	**5 out of 10**
$-8V_{dc}$	$-V_4-V_3+V_1$	0	1	1	0	0	1	0	1	1	0	**2 out of 4**	**5 out of 10**
$-9V_{dc}$	$-V_4-V_3$	1	0	0	0	0	1	0	1	1	0	**1 out of 4**	**4 out of 10**
$-10V_{dc}$	$-V_4-V_3-V_2$	0	1	0	1	0	1	0	1	1	0	**2 out of 4**	**5 out of 10**

TABLE II. CHARACTERISTICS OF THE PROPOSED MLI AND OTHER CONVERTERS

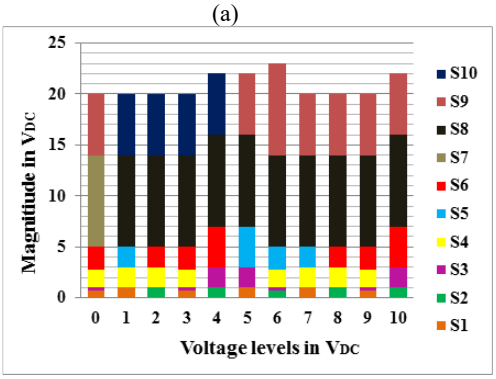
Parameters / References	Number of OVLs	Number of sources	Number of switches	Number of Gate-Drivers	Number of diodes	Number of capacitors	TSV($*V_{dc}$)
[13]	21	4	10	10	4	0	50
[14]	25	2	12	12	2	2	56
[15]	25	2	11	11	12	6	63
[16]	21	6	16	14	0	0	44
[17]	21	4	16	13	0	0	64
[18]	21	4	17	14	0	0	77
[18]	19	3	13	11	0	0	69
[19]	25	8	20	14	0	0	60
[22]	21	6	12	12	4	0	47
[26]	21	6	16	16	0	0	50
Proposed	21	4	14	10	0	0	44

MLIs, according to their structure, can generate various OVLs. For rational comparison, multilevel inverters which can produce 21 levels or near are chosen. Table II depicts the characteristics of the proposed MLI and some of the mentioned references.

According to information of Table II, reference [13] for producing 21 OVLs applies 4 fewer switches but needs 4 diodes and has a higher TSV. References [14] and [15] have higher TSV with higher OVLs, but there are more components. Just reference [16] has TSV= $44V_{dc}$, but it utilizes two switches and two sources more than the proposed MLI in 21 OVLs. Reference [17] uses more switches and gate driver circuits and has higher TSV. In reference [18], for generating 21 and 19 OVLs, the rate of TSV is higher than the proposed MLI which increases price and losses. Reference [22] in asymmetric configuration and 21 OVLs needs 4 diodes and 2 sources more than the proposed one and TSV is high. And reference [26] for 21 OVLs uses 2 sources, 2 switches and 6 Gate-Drivers more than the suggested converter. MLI with lower TSV in comparison with the proposed one generates lower OVLs. Switches are under various voltage stresses. Fig. 3 displays the voltage stress of each switch at different levels of the proposed 21 levels of MLI. In addition, the peak inverse voltage (PIV) of each switch is illustrated in Fig. 4. According to this picture, just two switches S_7 and S_8 have maximum PIV of 9 V_{dc} which is less than the maximum output voltage of $10V_{dc}$, and PIV of the others are noticeably lower. So, the proposed MLI has a low TSV that leads to lower price of switches and losses of switching. Fig. 5 shows the TSV of the proposed MLI with recently published converters under different OVLs based on V_{dc}, and Fig. 6 depicts a schematic comparison of the important parameters in the proposed MLI and others.



(a)



(b)

Fig. 3. Stress voltage of each switch at different levels of MLI at 21 OVLs. (a) negative levels, (b) zero, and positive levels.

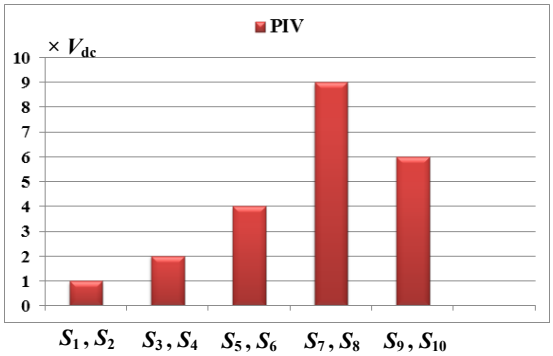


Fig. 4. PIV of each switch at the proposed MLI of 21 OVLs.

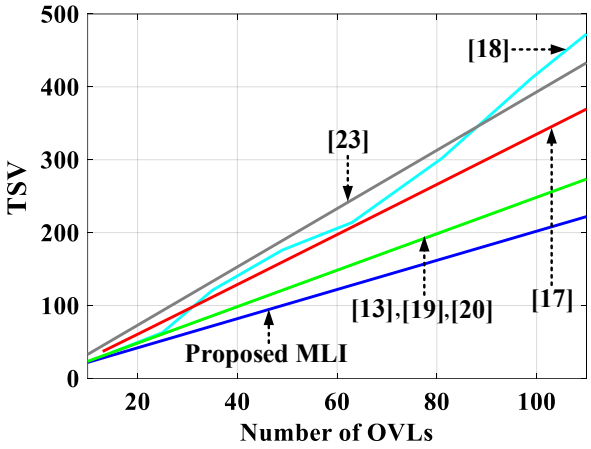


Fig. 5. TSV of the proposed MLI and other converters under different OVLs and base on V_{dc}.

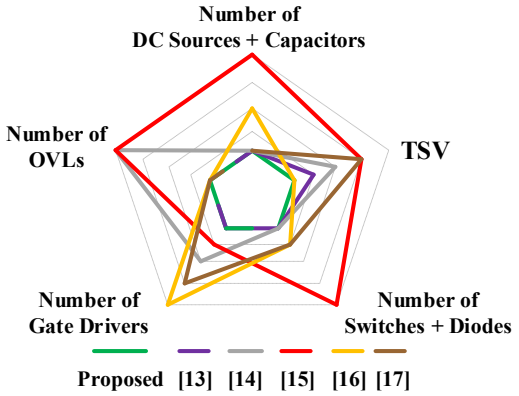


Fig. 6. Schematic comparison of parameters of the proposed and other MLIs.

3.1. Efficiency and power losses

The proposed multilevel inverter includes DC voltage sources and switches. So, losses happen just on switches in two parts: switching losses (P_{sw}) and conduction losses (P_{cu}). Switching losses consist of two parts too. The first part happens when switches are turned on and off because the current and voltage of the switches do not change abruptly. t_{rr} and t_{ff} are the duration of turning on and off the switches in order. The second part happens due to the output capacitance (C_{oss}) of the switches. When switches are connected, the conductive resistance of the switches or their parallel diodes and the voltage drop of them cause conductive losses.

3.1.1. Switching losses

Switching losses of each and total of switches are as below, where $V_{ds,n}$, $I_{av,n}$, and $f_{s,n}$ are voltage, average current, and frequency of the nth switch. k is the number of switches.

$$P_{sw,n}=\left(\frac{1}{2}\times V_{ds,n}\times I_{av,n}\times (t_{rr,n}+t_{ff,n})\times f_{s,n}\right)+\left(\frac{1}{2}\times C_{oss,n}\times f_{s,n}\times V_{ds,n}^{2}\right) \quad (8)$$

$$P_{sw,Total}=\sum_{n=1}^{k} P_{sw,n} \quad (9)$$

3.1.2. Conduction Losses

If $R_{ds,n}$ is considered conductive resistance of the nth switch or its parallel diode and also root mean square (RMS) current of the nth switch is supposed $I_{rms,n}$, conduction losses of the related switch will be as follow:

$$P_{cu,n}=(V_{ds,n}\times I_{av,n})+(R_{ds,n}\times I_{rms,n}^{2}) \quad (10)$$

Whereas there are two switches in the bidirectional switches, conduction losses of equation (10) for this kind of switches are considered double. Conduction losses of all switches are calculated by formula of (11).

$$P_{cu,Total}=\sum_{n=1}^{k} P_{cu,n} \quad (11)$$

Finally, the total losses of the proposed MLI are obtained as below:

$$P_{Losses}=P_{cu,Total}+P_{sw,Total} \quad (12)$$

4. Switching Strategy

Multilevel inverters consist of a significant number of switches, and how they are switched is very important to produce an output voltage close to a sine wave with low total harmonic distortion. The low THD causes no need or, if necessary, the need for a small filter to meet the standard of the Institute of Electrical and Electronics Engineering (IEEE). The THD value of the output voltage in multilevel inverters depends on the number of output voltage levels and how the converter is switched. So, at the same number of levels, the rate of harmonics entirely depends on the switching technique. There are different strategies for switching MLIs. In this part, the features of some of them are mentioned, and finally, a simple and useful strategy is proposed and used.

Level Shifted Sinusoidal Pulse With Modulation (LSSPWM) and Phase Shifted Sinusoidal Pulse With Modulation (PSSPWM) are the most basic and simple methods for switching. Each of these techniques includes a sinusoidal reference and several triangle carriers. The number of carriers completely depends on the number of OVLs. Carriers are set vertically over each other or horizontally side by side. By comparing the sine wave reference with the carriers, the level number and, thus, the state of the switches are determined. Implementation of these methods is simple, but due to the asymmetry of levels, THD is high. Also, additional and non-useful switching is done. Fig. 7 depicts the switching technique in SPWM methods. In these strategies for n OVLs, n-1 carriers are necessary.

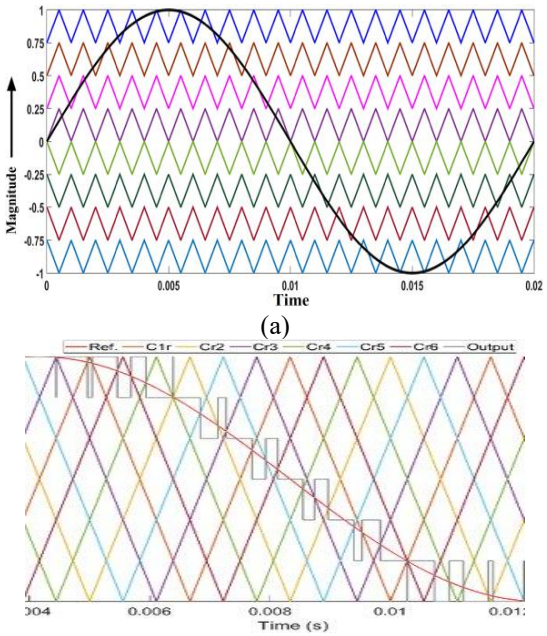


Fig. 7. Switching strategies in SPWM. (a) LSSPWM, (b) PSSPWM.

The authors in references [20] and [21] present a control and switching strategy for multilevel inverters as MP-NLC. This method needs the system model and related equations at the first step. Then, the authors define a cost function that consists of four sub-functions, such as optimal output voltage, limitation of filter current, elimination of non-optimal switching states, and source balancing. Implementation of this strategy is complicated, and high switching frequencies and THD are the main drawbacks.

Selected Harmonic Elimination Pulse with Modulation (SHE-PWM) and Selected Harmonic Mitigation Pulse with Modulation (SHM-PWM) are other switching techniques in MLIs. In this method, a Fourier analysis of the output voltage is done. By considering sinusoidal output voltage, just the odd sequence is studied as the below set of equations, where n is the harmonic order and θ_s represents the switching angle of the sth switch. Because of nonlinearity equations, some algorithms, such as particle swarm optimization (PSO) and genetic algorithm (GM) are applied to find the best angles [23]. So this technique is not easy to implement. In the SHE strategy, just a few defined low-order harmonics are eliminated instead of all harmonics distortion. g is the amplitude of the basic component of the output voltage[27].

$$\begin{aligned}
&\cos(\theta_1) + \cos(\theta_2) + \ldots + \cos(\theta_s) = g \\
&\cos(3\theta_1) + \cos(3\theta_2) + \ldots + \cos(3\theta_s) = 0 \\
&\cos(5\theta_1) + \cos(5\theta_2) + \ldots + \cos(5\theta_s) = 0 \\
&\qquad\qquad\vdots \\
&\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s) = 0
\end{aligned} \tag{13}$$

Another switching technique in multilevel inverters is hysteresis switching control. In this strategy, error (e) is an important parameter and is calculated by subtracting the output voltage from the reference voltage. Other parameters are δ and h. h is obtained based on the percentage of allowable error and δ is about 10% of h ($\delta \ll h$). U defines the number of voltage levels and squares according to Fig. 8. In this figure, the number of levels is nine. By comparing e with rates of δ and h, the corresponding level is obtained [25]. The high switching frequency is the main disadvantage of the hysteresis control.

Nearest Level Control (NLC) is similar to LSSPWM, but in this method, instead of triangle carriers, constant ones are chosen. Implementation of the suggested switching technique is easy and has efficient results. In the NLC switching strategy, the stepped output voltage is completely adapted to the sinusoidal reference. Therefore, the total harmonic decreases and meets IEEE standards. Fig 9 and 10 illustrate the flow chart technique and schematic of output and reference voltage under the NLC switching technique for 21 OVLs in order. $\boldsymbol{V_{ref}}$ and $\boldsymbol{V_o}$ are reference and output voltage, respectively.

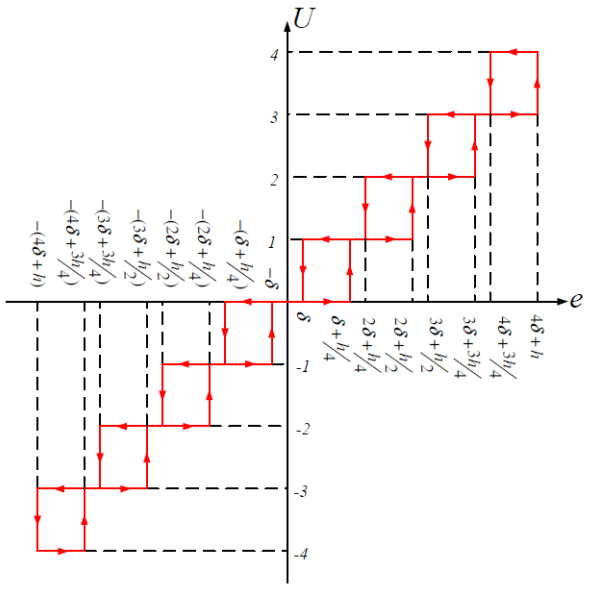


Fig. 8. Hysteresis diagram features of the hysteresis control in 9 OVLs.

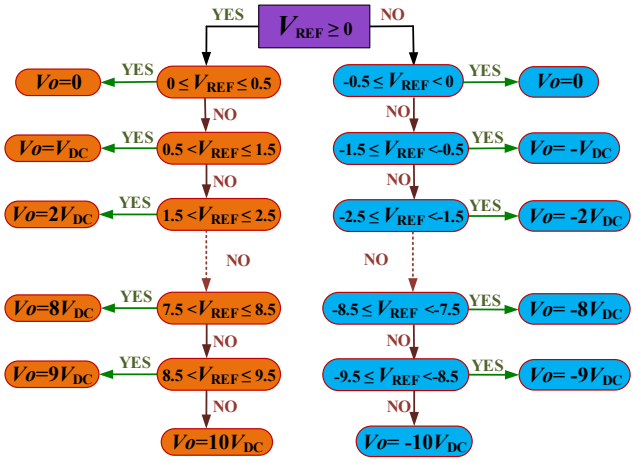


Fig. 9. Flow chart of NLC switching technique.

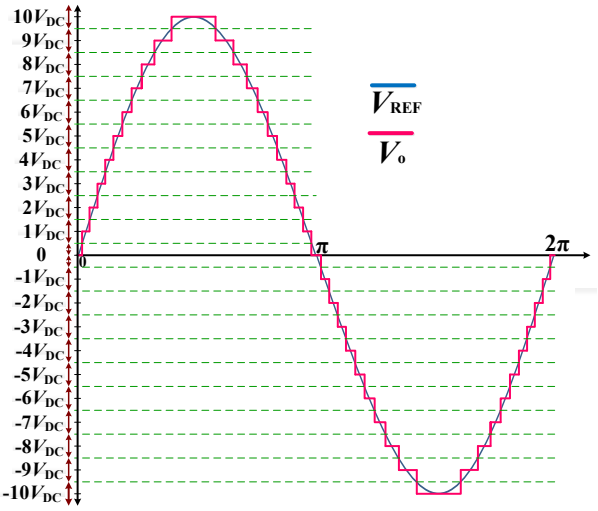


Fig. 10. Schematic of reference and output voltage under NLC switching method.

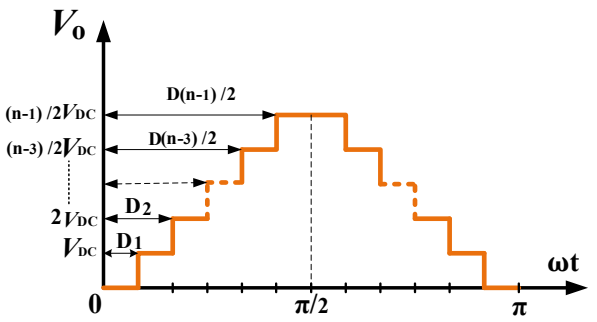


Fig. 11. Switching angels of a n-level MLI in half cycle.

Another switching strategy presented in [24] is Optimal Switching Angels (OSA). In this method for n OVLs, there are $\frac{(n-1)}{2}$ switching angles. These angles are investigated at the first quarter of the output voltage cycle for generating a symmetrical waveform, as shown in Fig. 11. In this strategy, there are just odd harmonics in the output voltage. The components of the output voltage based on Fourier analysis are as follows:

$$\begin{cases} V_{L1} = \sum_{i=1,3,5}^{\infty} \frac{4V_{dc}}{i\pi}\cos(iD_1) \\ V_{L2} = \sum_{i=1,3,5}^{\infty} \frac{4V_{dc}}{i\pi}\cos(iD_2) \\ \vdots \\ V_{L(\frac{n-1}{2})} = \sum_{i=1,3,5}^{\infty} \frac{4V_{dc}}{i\pi}\cos\left(iD_{(\frac{n-1}{2})}\right) \end{cases} \quad (14)$$

$$\boldsymbol{V_{out} = V_{L1} + V_{L2} + \ldots + V_{L(\frac{n-1}{2})}} \quad (15)$$

V_{Li} is the voltage of ith level and V_{out} is the output voltage. D_1, D_2, … and $D_{(\frac{n-1}{2})}$ are switching angels of first, second and, $(\frac{n-1}{2})^{th}$ level in order. The THD formula is nonlinear and is supposed as a cost function. So, a PSO algorithm is used to minimize THD by choosing optimized switching angels. In this strategy, an inequality of $0 < D_1 < D_2 < \ldots < D_{(\frac{n-1}{2})}$ should be met. By minimizing THD, optimal switching angels are calculated from equation (16) [28].

$$\boldsymbol{D_i = \sin^{-1}(\frac{i-0.5}{\frac{n-1}{2}})} \quad \text{for} \quad i = 1, 2, 3, \ldots, \frac{n-1}{2}. \quad (16)$$

The optimal switching angles are obtained when the staircase quasi-sinusoidal output voltage best matches the ideal reference waveform. In OSA Method, the optimal switching angle is determined using (14) to (16) equations. In NLC technique, the same optimal switching angles are obtained by comparing the ideal reference waveform with predefined threshold values, which are determined based on the output voltage levels (as shown in Fig. 10). Consequently, both methods produce identical output waveforms.

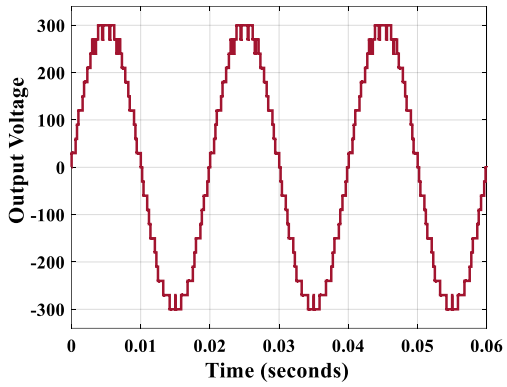
5. Simulation Results

To make sure of the correct operation of the proposed MLI, first, according to the parameters of Table III a prototype is simulated in MATLAB/SIMULINK. The proposed converter can work under load with a power factor of less than one. In this situation, for a short time of each period, the current and voltage of the load have different polarities. At this time, current passes through the diodes of switches. The simulation is done under four switching techniques: LSSPWM, Hysteresis, NLC, or OSA. V_{omax} is the maximum output voltage. Fig. 12 shows the output voltage and its THD in the proposed MLI under the LSSPWM switching strategy. Fig. 13 displays the output voltage and related THD of the proposed MLI under the hysteresis switching technique for δ=0.5 and h=5. The results of output voltage under NLC and OAS switching techniques are the same. Fig. 14 (a) and (b) depict output voltage and related THD under the NLC or OSA switching strategy in order. As shown in Figures 12(b), 13(b), and 14(b), the output voltage THD over three cycles (up to 0.06 seconds) is 4.84%, 2.79%, and 2.38%, respectively. Based on these results, the NLC or OSA switching techniques exhibit the lowest output voltage harmonic distortion. In addition to low THD, the mentioned switching strategies (NLC or OSA) offer the advantages of a low switching frequency and a high output voltage of fundamental component.

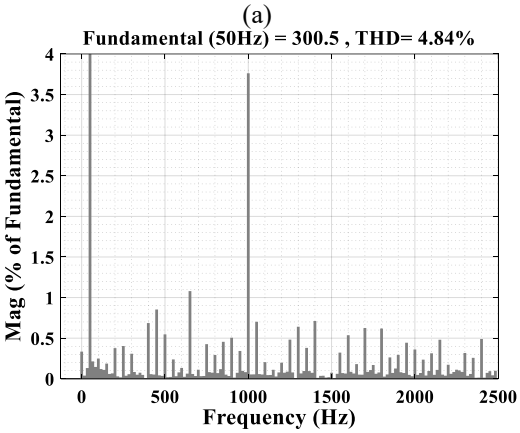
According to equation of (16), 10 optimal switching angels of the 21-OVLs proposed MLI are listed in Table IV. Fig. 15 illustrates a half-cycle of output voltage under the OSA switching method with the optimal angels.

TABLE III. Parameters of the Proposed MLI in Simulation.

Parameters	Value
Number of OVLs	21
$\boldsymbol{V_{dc}}$	30V
$\boldsymbol{V_{omax}}$ & $\boldsymbol{V_{orms}}$	300V & 213V
Number of DC sources	4
Number of GDs	10
Number of switches	14
Output frequency	50 Hz
$\boldsymbol{P_{Load}}$	216W
$\boldsymbol{R_{Load}}$ & $\boldsymbol{L_{Load}}$	210Ω & 10.2mH

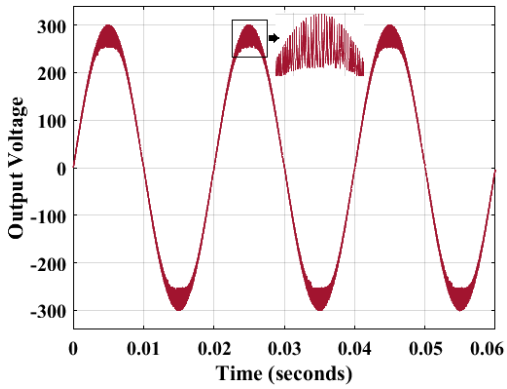


(a)

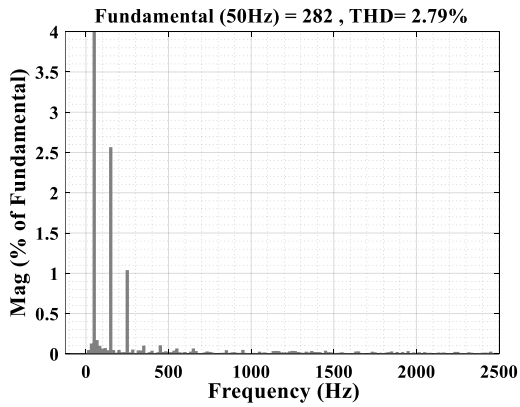


(b)

Fig. 12. Output voltage of the proposed MLI under LSSPWM switching. (a) Output voltage, (b) THD of output voltage.

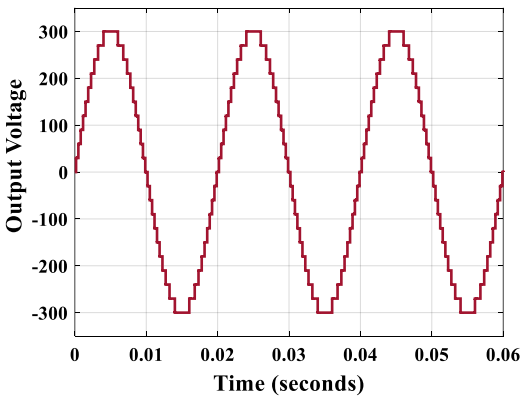


(a)

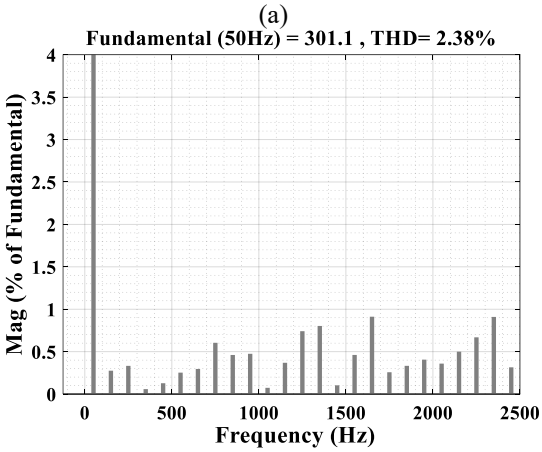


(b)

Fig. 13. Output voltage of the proposed MLI under Hysteresis switching. (a) Output voltage, (b) THD of output voltage.



(a)



(b)

Fig. 14. Output voltage of the proposed MLI under NLC or OSA switching. (a) Output voltage, (b) THD of output voltage.

TABEL IV. 10 OPTIMAL SWITCHING ANGEL IN 21-OVLS.

Angels (OSA Based)	D_1	D_2	D_3	D_4	D_5	THD_V
Degree	2.866	8.27	14.47	20.48	26.74	
Angels (OSA Based)	D_6	D_7	D_8	D_9	D_{10}	2.38%
Degree	33.37	40.54	48.59	58.21	71.8	

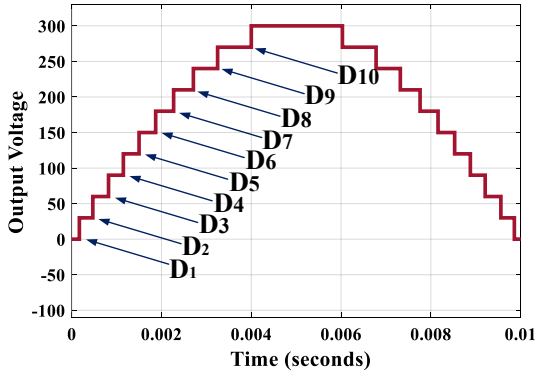


Fig. 15. Half cycle of output voltage under optimal switching angel.

As they are observed, THD in the LSSPWM method is high, and there is some extra and useless switching. THD in hysteresis switching is proper and better than LSSPWM, but the switching frequency is noticeably high, and applying a filter, consisting of an inductor and a capacitor, is necessary. In addition, because of the defined allowable percentage error, the fundamental voltage is low. The THD of output voltage in NLC and OSA

switching strategies without any filter is perfect. Also, the average switching frequency is lower than others.

5.1. Efficiency

By considering equations [8-12] and information in the datasheet of MOSFET IRFP460, as it is used for all of the switches in the experimental part, and under the operation of Table III and NLC switching pattern, efficiency of the proposed MLI is obtained versus of the output power and based on Watt (W), as illustrated in Fig. 16. As it is observed, switching losses are negligible, and all of the losses belong to conduction. Losses of each switch in 216W output power (rate of laboratory prototype) are displayed in Fig. 17.

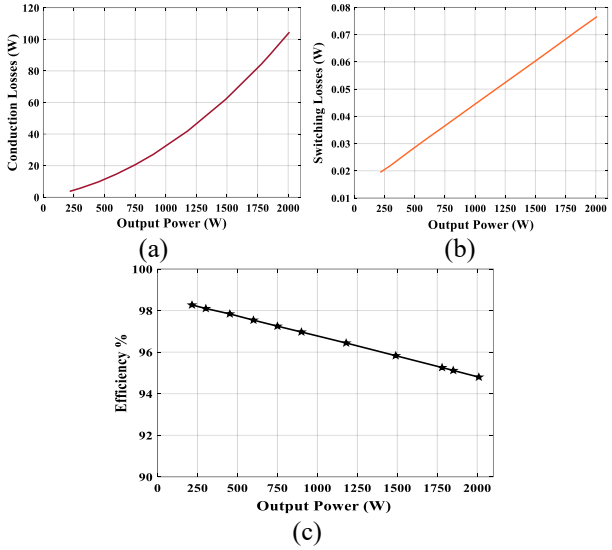


Fig. 16. Losses and efficiency of the proposed MLI versus output power. (a) Conduction Losses, (b) Switching Losses, (c) Efficiency.

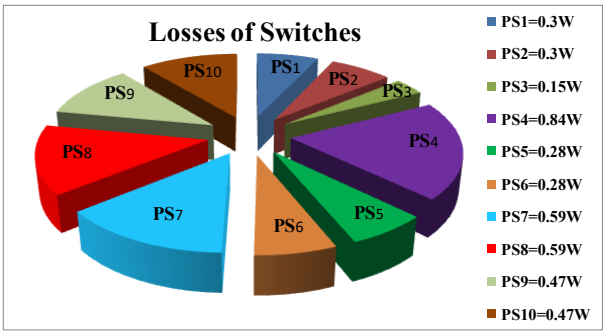


Fig. 17. Switches losses of the proposed 21-level MLI in 216W output power.

6. Experimental Results

To prove the correct operation of the proposed MLI, a prototype with 216W power is generated in the lab. The characteristics of the prototype are the same as Table III and other features are according to Table V. Fig. 18 shows the setup of the proposed MLI in the laboratory. Fig. 19 (a) and (b) depict the output voltage in one cycle and the output voltage and current of the proposed MLI together under the NLC switching strategy in order. Fig. 19 (c) shows the output voltage and current of the proposed converter under the LSSPWM switching strategy. Under operation of the proposed MLI, according to the parameters of Table V and NLC switching pattern, stress voltage of switches are as shown in Fig. 19 (d) to 19 (i). While switches (S_1, S_2), (S_5, S_6), (S_7, S_8) and (S_9, S_{10}) are switched complementary, the value of stress voltage is the same. Switches S_3 and S_4 are operated independently. According to equation (7) and the value of DC sources from Table V, TSV is 1320V for this test. Switches are trigged under the NLC and LSSPWM switching techniques by the DSP microcontroller. Similar results from the experimental prototype and simulation prove the appropriate operation of the proposed MLI.

Table V. Features of the proposed MLI in the experimental sample.

Parameters	Rate or Kind
Microcontroller	*DSP-TMS320-F28335*
Gate-Driver	*TC4420 & TLP250H*
Switches	*IRFP 460*
Value of DC sources	*30,30,90,180V*
Output Frequency	*50Hz*
Carrier Frequency (in LSSPWM)	*1.25KHz*
Power	*216W*
R&L (Load)	*210Ω, 10.2mH*

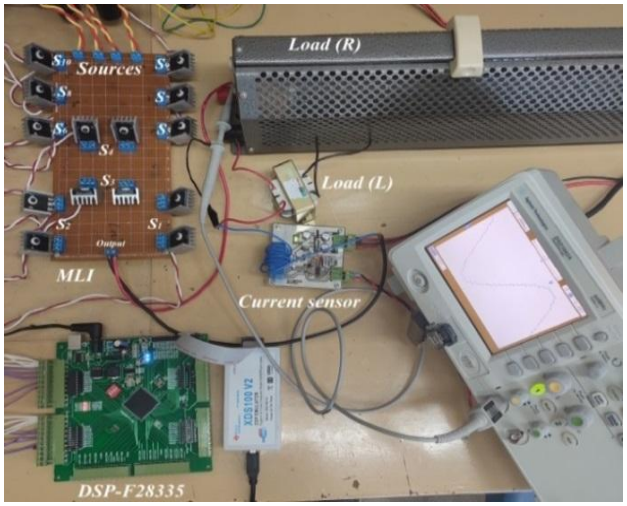


Fig. 18. Setup of the proposed MLI in the Lab.

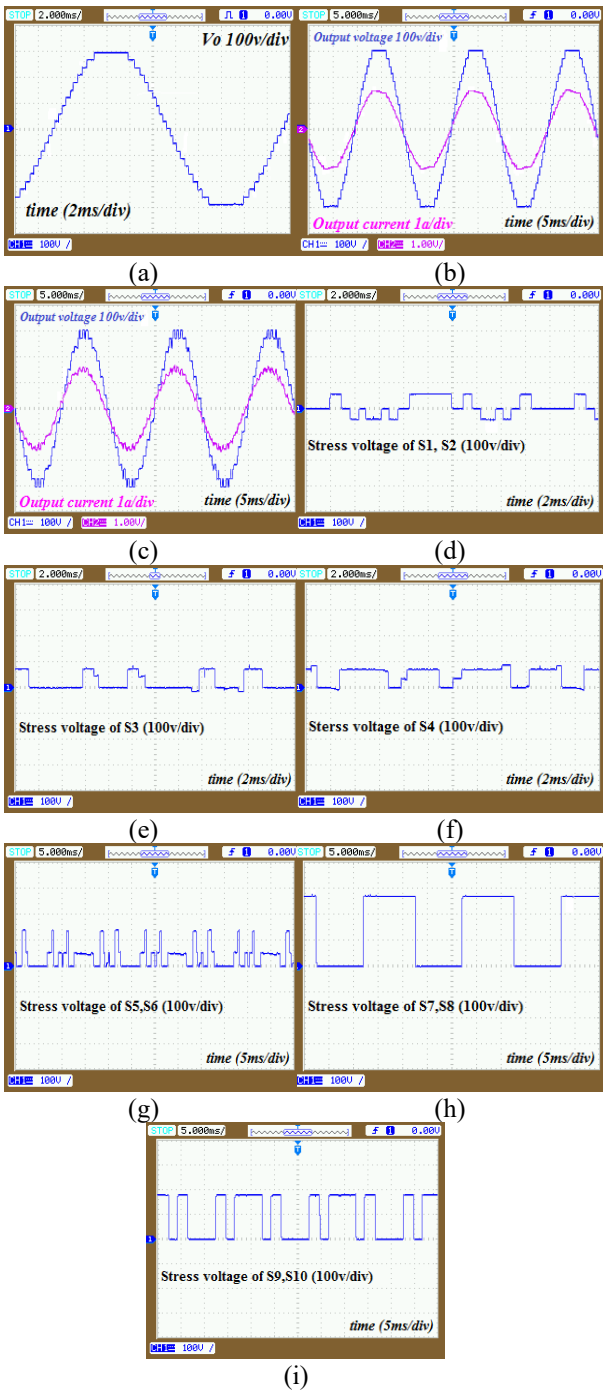


Fig. 19. Output results of the proposed MLI in 21-OVLs under NLC and LSSPWM switching technique, and stress voltage of switches under NLC switching strategy. (a) One cycle output voltage under NLC switching technique, (b) Output voltage and current under NLC switching technique, (c) Output voltage and current under LSSPWM switching strategy, (d) Stress voltage of S_1 and S_2, (e) Stress voltage of S_3, (f) Stress voltage of S_4, (g) Stress voltage of S_5 and S_6, (h) Stress voltage of S_7 and S_8, and, (i) Stress voltage of S_9 and S_{10}.

Fig. 20 displays the efficiency of the proposed MLI in the experimental investigation and in the range of 50 to 200W. As it is observed, efficiency is 97.5% for 50W and 96.7% for 200W power. By raising power, conduction losses increase too, which decreasing efficiency. Fig. 21 illustrates the experimental harmonic spectrum of the output voltage of the proposed MLI in 21-OVLs under NLC and LSSPWM switching techniques.

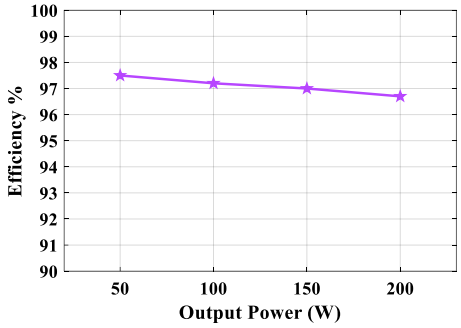


Fig. 20. Efficiency of the experimental proposed MLI under different power.

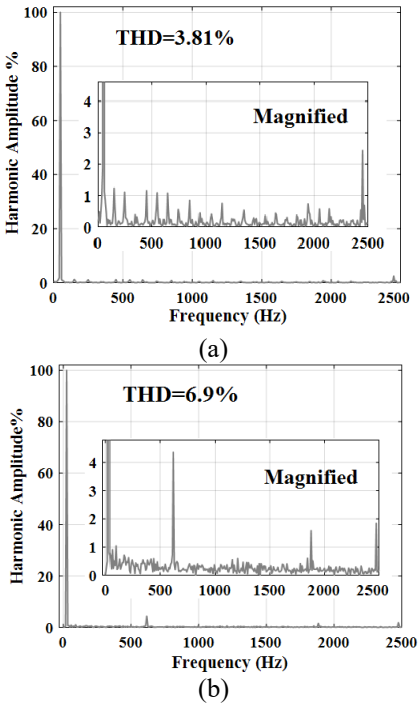


Fig. 21. Experimental harmonic spectrum of 21 output voltage levels in the suggested MLI. (a) Under NLC switching, (b) Under LSSPWM switching technique.

7. Conclusion

This paper studied several common switching techniques of MLIs and applied some of them on the proposed asymmetrical multilevel inverter with the features of low TSV, simple extendibility and a proper number of components and efficiency. The suggested MLI was analysed and compared with other structures. Several common switching techniques were mentioned, and some of them were simulated and compared with each other. Finally, NLC or OSA and LSSPWM strategies with simple implementation and proper outcomes (low THD and switching frequency) were chosen for the proposed multilevel inverter. First, for validation, the proposed MLI with 21 OVLs was simulated in MATLAB/SIMULINK. Then, a 216W prototype was generated in the lab. Results verify the correct and proper operation of the suggested MLI.

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